Chettinad
College of Engineering & Technology
Approved by AICTE-New Delhi and Affiliated to Anna University-Chennai

DEPARTMENT OF

ELECTRICAL AND ELECTRONICS ENGINEERING

EE3412 LINEAR AND DIGITAL CIRCUITS LABORATORY

2021 REGULATION

(As per ANNA University)

OBSERVATION RECORD

Name of the student : _____

Register Number : _____

Year/ Semester/ section: _____

CHETTINAD COLLEGE OF ENGINEERING AND TECHNOLOGY

(Puliyur, Karur – 639114)

Program Outcomes (POs) **Electrical and Electronics Engineering Graduates will be able to:**	
PO1	**Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
PO2	**Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
PO3	**Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
PO4	**Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
PO5	**Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations
PO6	**The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
PO7	**Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
PO8	**Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
PO9	**Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
PO10	**Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

Program Outcomes (POs) **Electrical and Electronics Engineering Graduates will be able to:**	
PO11	**Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
PO12	**Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.
Program Specific Outcomes (PSO)	
PSO1	Foundation of Electrical Engineering: Ability to understand the principles and working of electrical components, circuits, systems and control that are forming a part of power generation, transmission, distribution, utilization, conservation and energy saving. Students can assess the power management, auditing, crisis and energy saving aspects.
PSO2	Foundation of Mathematical Concepts: Ability to apply mathematical methodologies to solve problems related with electrical engineering using appropriate engineering tools and algorithms
PSO3	Computing and Research Ability: Ability to use knowledge in various domains to identify research gaps and hence to provide solution which leads to new ideas and innovations

EE3412 LINEAR AND DIGITAL CIRCUITS LABORATORY L T P C
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COURSE OBJECTIVES:

- To learn design, testing and characterizing of circuit behavior with combinational logic gate ICs.
- To learn design, testing and characterizing of circuit behavior with register/ counter and sequential logic ICs.
- To learn design, testing and characterizing of circuit behavior with OPAMP ICs.
- To learn design, testing and characterizing of circuit behavior with analog Ics like 555 timer VCO and regulators.
- To learn design, testing and characterizing of circuit behavior with digital Ics like decoders, Multiplexers

LIST OF EXPERIMENTS:

1. Implementation of Boolean Functions, Adder and Subtractor circuits.
2. Code converters: Excess-3 to BCD and Binary to Gray code converter and vice-versa.
3. Parity generator and parity checking.
4. Encoders and Decoders.
5. Counters: Design and implementation of 3-bit modulo counters as synchronous and Asynchronous types using FF IC's and specific counter IC.
6. Shift Registers: Design and implementation of 4-bit shift registers in SISO, SIPO, PISO, PIPO modes using suitability IC's.
7. Study of multiplexer and de multiplexer
8. Timer IC application: Study of NE/SE 555 timer in Astability, Monostability operation.
9. Application of Op-Amp: inverting and non-inverting amplifier, Adder, comparator, Integrator and Differentiator.
10. Voltage to frequency characteristics of NE/ SE 566 IC.
11. Variability Voltage Regulator using IC LM317.

TOTAL: 45 PERIODS

COURSE OUTCOMES:

At the end of the course the students will be able to

CO1: Ability to understand and implement Boolean Functions.

CO2: Ability to understand the importance of code conversion

CO3: Ability to Design and implement circuits with digital ICs like decoders, multiplexers, register.

CO4: Ability to acquire knowledge on Application of Op-Amp

CO5: Ability to Design and implement counters using analog ICs like timers, VCOs and digital ICs like Flip-flops and counters.

LIST OF EXPERIMENTS

EX.No	Name of the Experiment	Page No
1	Implementation of Boolean Functions, Adder and Subtractor circuits.	
2	Code converters: Excess-3 to BCD and Binary to Gray code converter and vice-versa.	
3	Parity generator and parity checking.	
4	Encoders and Decoders	
5	Counters: Design and implementation of 3-bit modulo counters as synchronous and Asynchronous types using FF IC's and specific counter IC.	
6	Shift Registers: Design and implementation of 4-bit shift registers in SISO, SIPO, PISO, PIPO modes using Suitability IC's.	
7	Study of multiplexer and de multiplexer	
8	Timer IC application: Study of NE/SE 555 timer in stability, Monostability operation.	
9	Application of Op-Amp: inverting and non-inverting amplifier, Adder, comparator, Integrator and Differentiator.	
10	Voltage to frequency characteristics of NE/ SE 566 IC	
11	Variability Voltage Regulator using IC LM31	
VALUE ADDED EXPERIMENTS		
1	Design and implementation of Instrumentation amplifier using IC741	
2	**SIMULATION USING SPICE :**Bistable Multivibrator	

Ex.No:1(a) IMPLEMENTATION OF BOOLEAN FUNCTIONS

Date:

AIM:

To design the logic circuit and verify the truth table of the given Boolean logic gates.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Digital IC trainer kit		1
2.	AND gate	IC 7408	1
3.	OR gate	IC 7432	1
4.	NOT gate	IC 7404	1
5.	NAND gate	IC 7400	1
6.	NOR gate	IC 7402	1
7.	EX-OR gate	IC 7486	1
8.	Connecting wires		As required

PRE-LAB QUESTIONS:

1. What is a Boolean function?
2. What are the different ways to represent a Boolean function?
3. What is the canonical form of a Boolean function?
4. What are logic gates? Name the basic logic gates.
5. What is the canonical form of a Boolean function?

THEORY:

- Circuit that takes the logical decision and the process are called logic gates.
- Each gate has one or more input and only one output.
- OR, AND and NOT are basic gates. NAND, NOR and X-OR are known as universal gates. Basic gates form these gates.

AND GATE:

The AND gate performs a logical multiplication commonly known as AND function. The output is high when both the inputs are high. The output is low level when any one of the inputs is low.

OR GATE:

The OR gate performs a logical addition commonly known as OR function. The output is high when any one of the inputs is high. The output is low level when both the inputs are low.

NOT GATE:

The NOT gate is called an inverter. The output is high when the input is low.

The output is low when the input is high.

AND GATE:

The NAND gate is a contraction of AND-NOT. The output is high when both inputs are low and any one of the input is low .The output is low level when both inputs are high.

NOR GATE:

The NOR gate is a contraction of OR-NOT. The output is high when both inputs are low. The output is low when one or both inputs are high.

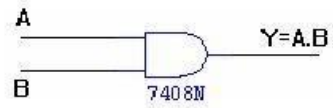
X-OR GATE:

The output is high when any one of the inputs is high. The output is low when both the inputs are low and both the inputs are high.

CIRCUIT DIAGRAM

AND GATE

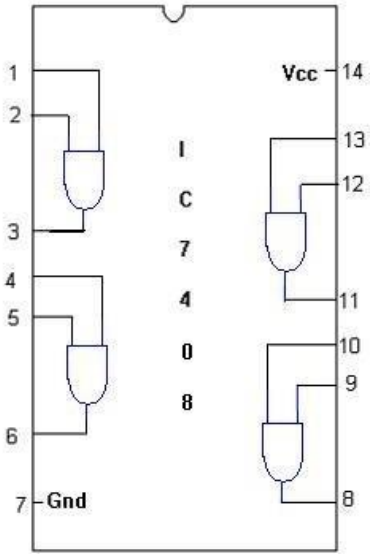
SYMBOL



TRUTH TABLE

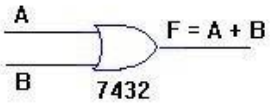
A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

PIN DIAGRAM

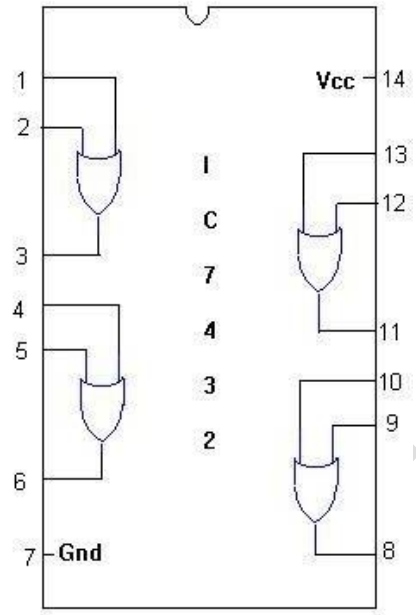


OR GATE

SYMBOL :



PIN DIAGRAM :



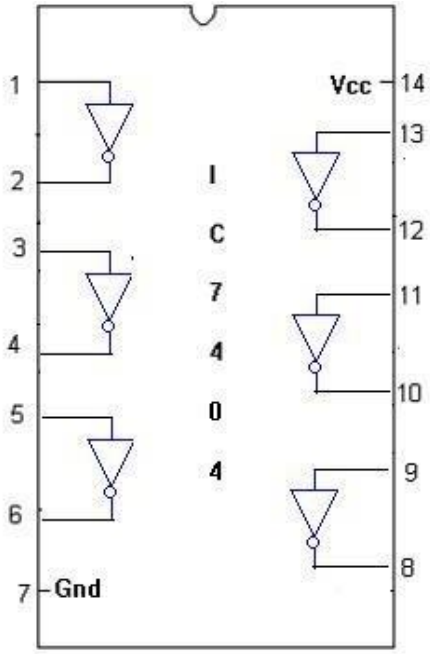
TRUTH TABLE

A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

NOT GATE

SYMBOL

PIN DIAGRAM

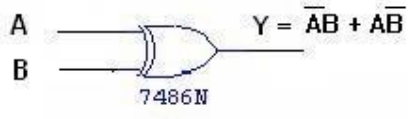


TRUTH TABLE :

A	$\overline{A}$
0	1
1	0

EX-OR GATE

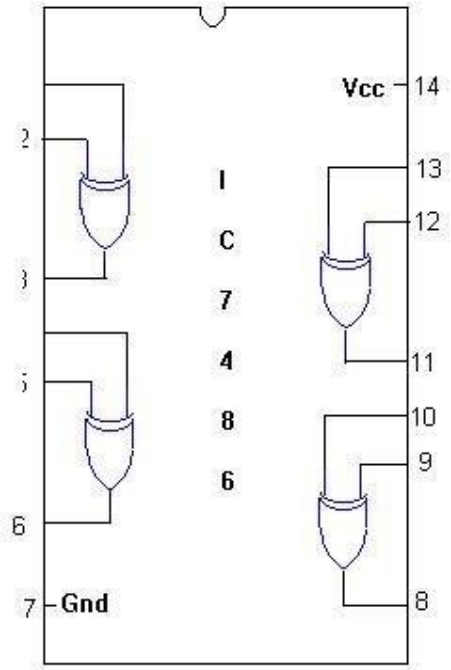
SYMBOL



TRUTH TABLE :

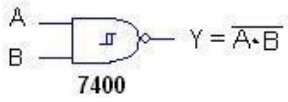
A	B	$\overline{A}B + A\overline{B}$
0	0	0
0	1	1
1	0	1
1	1	0

PIN DIAGRAM



2-INPUT NAND GATE

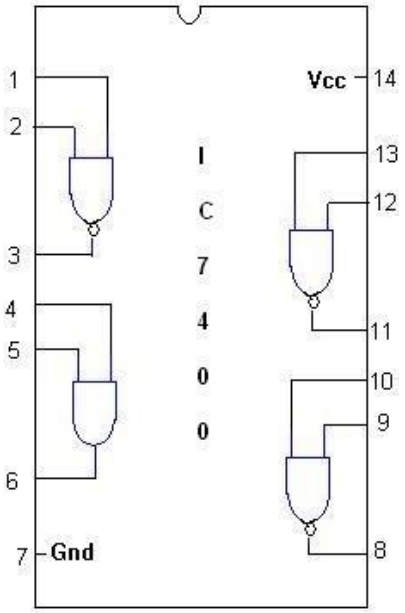
SYMBOL



TRUTH TABLE

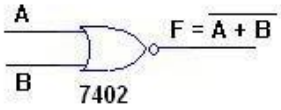
A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

PIN DIAGRAM

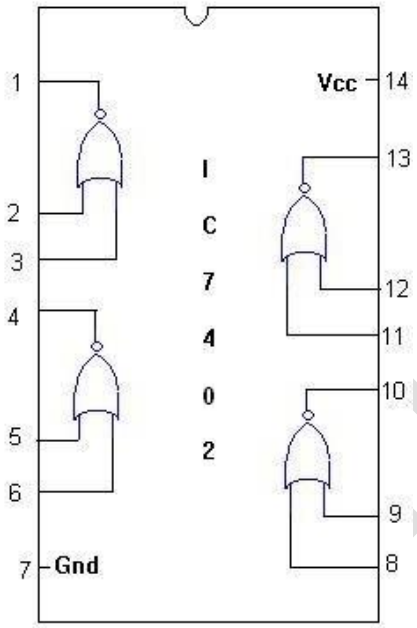


NOR GATE

SYMBOL :



PIN DIAGRAM :



TRUTH TABLE

A	B	$\overline{A+B}$
0	0	1
0	1	1
1	0	1
1	1	0

TRUTH TABLE:

S.No	INPUT				OUTPUT
	A	B	C	D	F=D'B'+C'(B'+A'D)
1.	0	0	0	0	1
2.	0	0	0	1	1
3.	0	0	1	0	1
4.	0	0	1	1	0
5.	0	1	0	0	0
6.	0	1	0	1	1
7.	0	1	1	0	0
8.	0	1	1	1	0
9.	1	0	0	0	1
10.	1	0	0	1	1
11.	1	0	1	0	1
12.	1	0	1	1	0
13.	1	1	0	0	0
14.	1	1	0	1	0
15.	1	1	1	0	0
16.	1	1	1	1	0

PROCEDURE:

1. Connections are given as per the circuit diagram
2. For all the ICs 7^{th} pin is grounded and 14^{th} pin is given +5 V supply.
3. Apply the inputs and verify the truth table for the given Boolean expression.

POST LAB QUESTIONS:

1. What is the difference between Sum of Products (SOP) and Product of Sums (POS)?
2. What are minterms and maxterms?
3. How do you convert a Boolean function into its SOP or POS form?
4. What are the rules for grouping cells in a K-map?
5. What are the different methods to simplify a Boolean function?

RESULT:

The truth table of the given Boolean expression was verified

Ex.No:1(b) DESIGN AND IMPLEMENTATION OF DDER/SUBTRACTOR

Date:

AIM:

To design and construct half adder, full adder, half subtractor and full subtractor circuits and verify the truth table using logic gates.

APPARATUS REQUIRED:

S. No	Name	Specification	Quantity
1.	IC	7432, 7408, 7486, 7483	1
2.	Digital IC Trainer Kit		1
3.	Patch chords		As required

PRE LAB QUESTIONS:

1. What is an adder?
2. What is the difference between a Half Adder and a Full Adder?
3. What are the inputs and outputs of a Half Adder?
4. What is the difference between a Half Subtractor and a Full Subtractor?
5. What are the inputs and outputs of a Half Subtractor?

THEORY:

The most basic arithmetic operation is the addition of two binary digits. There are four possible elementary operations, namely,

$$0 + 0 = 0$$

$$0 + 1 = 1$$

$$1 + 0 = 1$$

$$1 + 1 = 10$$

The first three operations produce a sum of whose length is one digit, but when the last operation is performed the sum is two digits. The higher significant bit of this result is called a carry and lower significant bit is called the sum.

HALFADDER:

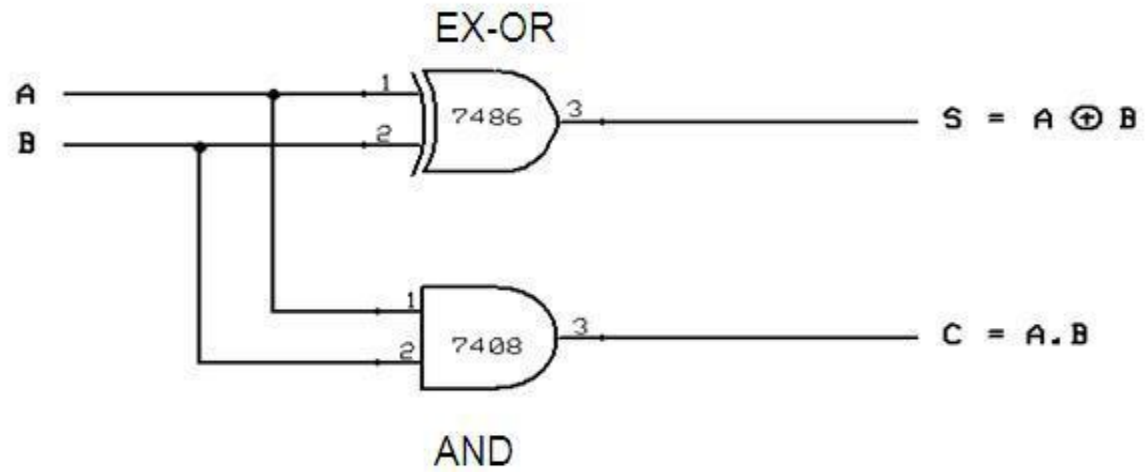
A combinational circuit which performs the addition of two bits is called half adder. The input variables designate the augend and the addend bit, whereas the output variables produce the sum and carry bits.

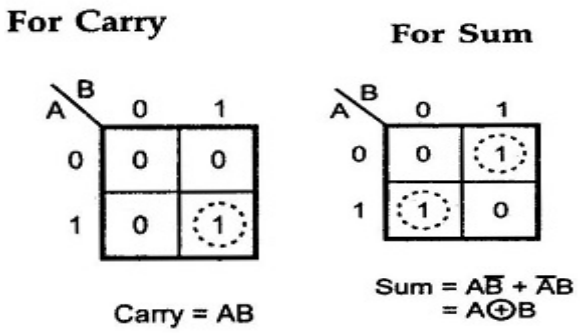
HALFADDER

TRUTH TABLE:

S.No	INPUT		OUTPUT	
	A	B	S	C
1.	0	0	0	0
2.	0	1	1	0
3.	1	0	1	0
4.	1	1	0	1

CIRCUIT DIAGRAM:





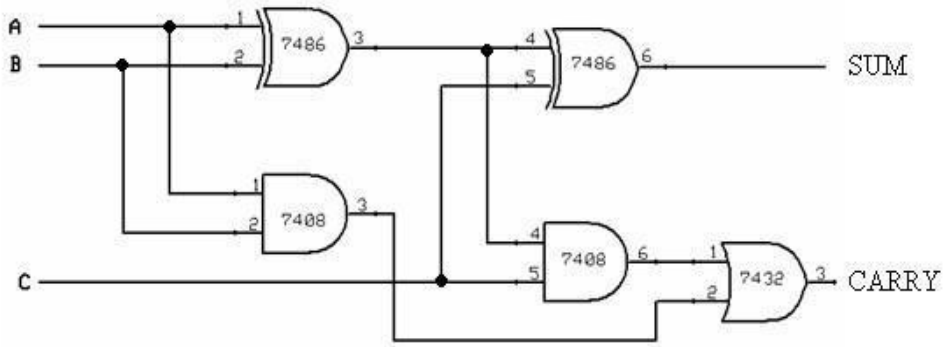
FULL ADDER

A combinational circuit which performs the arithmetic sum of three input bits is called full adder. The three input bits include two significant bits and a previous carry bit. A full adder circuit can be implemented with two half adders and one OR gate.

TRUTH TABLE:

S.No	INPUT			OUTPUT	
	A	B	C	SUM	CARRY
1.	0	0	0	0	0
2.	0	0	1	1	0
3.	0	1	0	1	0
4.	0	1	1	0	1
5.	1	0	0	1	0
6.	1	0	1	0	1
7.	1	1	0	0	1
8.	1	1	1	1	1

CIRCUIT DIAGRAM



SUM

A \ BC	B'C'	B'C	BC	BC'
A'	0	(1)	0	(1)
A	(1)	0	(1)	0

A \ BC	B'C'	B'C	BC	BC'
A'	0	(1)	0	(1)
A	(1)	0	(1)	0

A \ BC	B'C'	B'C	BC	BC'
A'	0	0	1	0
A	0	1	1	1

CARRY

A \ BC	B'C'	B'C	BC	BC'
A'	0	0	1	0
A	0	1	1	1

SUM = A'B'C + A'BC' + AB'C' + ABC = A ⊕ B ⊕ C

CARRY = AB + AC + BC

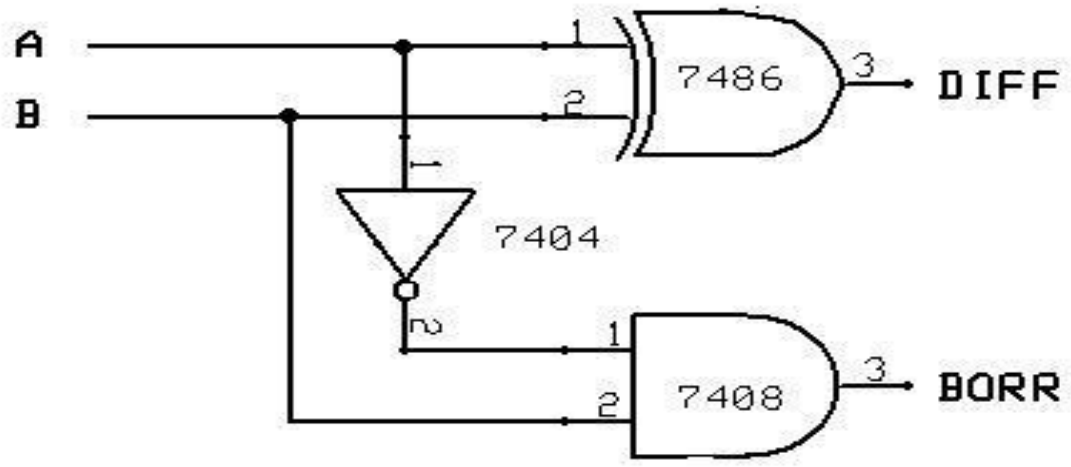
HALF SUBTRACTOR

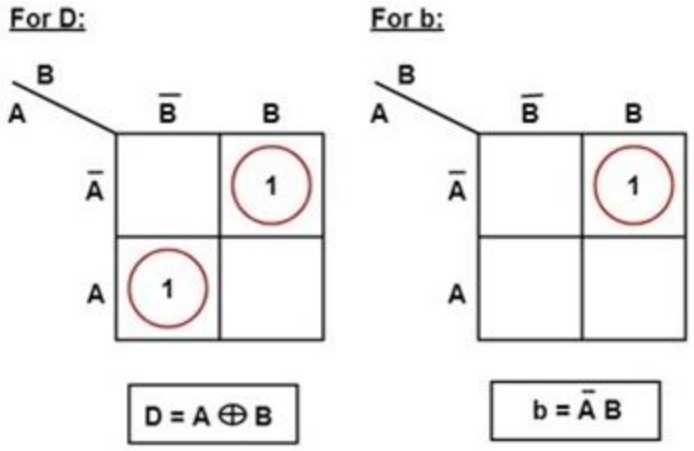
A combinational circuit which performs the subtraction of two bits is called half subtractor. The input variables designate the minuend and the subtrahend bit, whereas the output variables produce the difference and borrow bits.

TRUTH TABLE:

S.No	INPUT		OUTPUT	
	A	B	DIFF	BORR
1.	0	0	0	0
2.	0	1	1	1
3.	1	0	1	0
4.	1	1	0	0

CIRCUIT DIAGRAM:





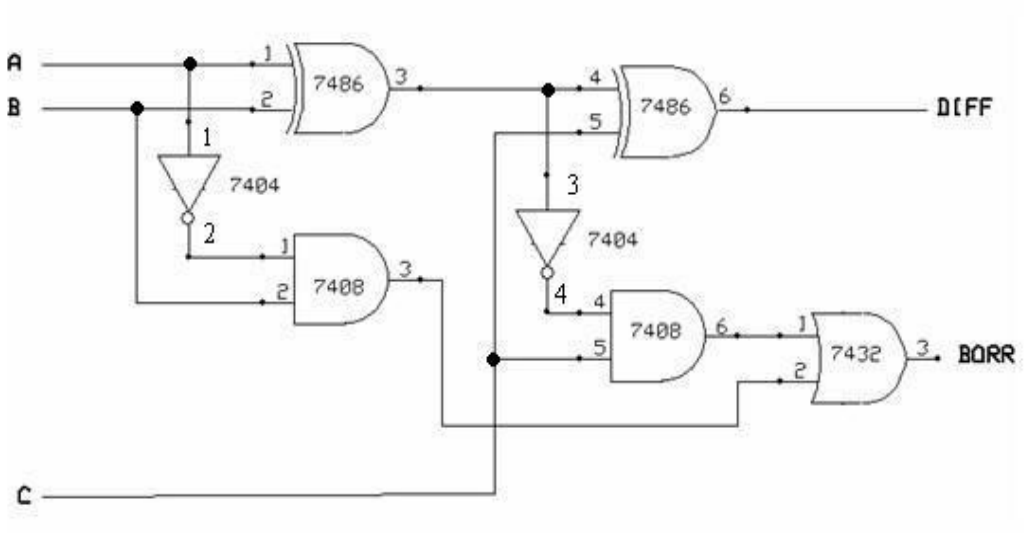
FULL SUBTRACTOR:

A combinational circuit which performs the subtraction of three input bits is called full subtractor. The three input bits include two significant bits and a previous borrow bit. A full subtractor circuit can be implemented with two half subtractors and one OR gate.

TRUTH TABLE:

A	B	B_{in}	D	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

CIRCUIT DIAGRAM:



DIFFERENCE

A \ BC	B'C'	B'C	BC	BC'
A'	0	(1)	0	(1)
A	(1)	0	(1)	0

A'B'C + A'BC' + AB'C' + ABC = A ⊕ B ⊕ C

BORROW

A \ BC	B'C'	B'C	BC	BC'
A'	0	(1	1)	1
A	0	0	1	0

BORROW = A'B + A'C + BC

PROCEDURE:

1. The connections are given as per the circuit diagram.
2. Two 4 – bit numbers added or subtracted depend upon the control input and the output is obtained.
3. Apply the inputs and verify the truth table for the half adder or s subtractor and full adder or subtractor circuits.

POST LAB QUESTIONS :

1. Can a Half Subtractor handle borrow from a previous stage? Why or why not?
2. Why is a Full Subtractor required instead of a Half Subtractor?
3. What is the advantage of using a Full Adder over a Half Adder?
4. How many Half Adders are required to design a Full Adder?
5. Which logic gates are used to implement a Half Adder?

RESULT:

Thus the half adder, full adder, half subtractor and full subtractor circuits were designed and their truth table were verified.

PARITY GENERATOR & CHECKER

Ex. No:2

Date:

AIM:

To design and verify the truth table of a three bit Odd Parity generator and checker & Even Parity Generator And Checker.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Digital IC trainer kit		1
2.	EX-OR gate	IC 7486	
3.	NOT gate	IC 7404	
4.	Connecting wires		As required

PRELAB QUESTIONS:

1. What is parity in digital systems?
2. What are the two types of parity?
3. What is the difference between a parity generator and a parity checker?
4. Why is parity checking used in data transmission?
5. What is an even parity generator?

THEORY:

A parity bit is used for the purpose of detecting errors during transmission of binary information. A parity bit is an extra bit included with a binary message to make the number of 1's either odd or even. The message including the parity bit is transmitted and then checked at the receiving end for errors. An error is detected if the checked parity does not correspond with the one transmitted. The circuit that generates the parity bit in the transmitter is called a parity generator and the circuit that checks the parity in the receiver is called a parity checker.

In even parity the added parity bit will make the total number of 1's an even amount and in odd parity the added parity bit will make the total number of 1's an odd amount.

In a three bit odd parity generator the three bits in the message together with the parity bit are transmitted to their destination, where they are applied to the parity checker circuit. The parity checker circuit checks for possible errors in the transmission.

Since the information was transmitted with odd parity the four bits received must have an odd number of 1's. An error occurs during the transmission if the four bits received have an even number of 1's, indicating that one bit has changed during transmission. The output of the parity checker is denoted by PEC (parity error check) and it will be equal to 1 if an error occurs, i.e., if the four bits received has an even number of 1's.

PARITYGENERATOR

TRUTH TABLE:

S.No	INPUT (Three bit message)			OUTPUT (Odd Parity bit)	OUTPUT (Even Parity bit)
	A	B	C	P	P
1.	0	0	0	1	0
2.	0	0	1	0	1
3.	0	1	0	0	1
4.	0	1	1	1	0
5.	1	0	0	0	1
6.	1	0	1	1	0
7.	1	1	0	1	0
8.	1	1	1	0	1

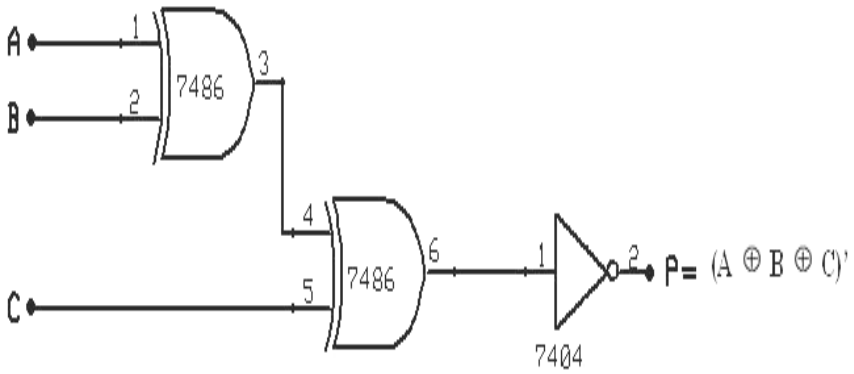
From the truth table the expression for the output parity bit is, $P(A, B, C) = \Sigma (0, 3, 5, 6)$

Also written as,

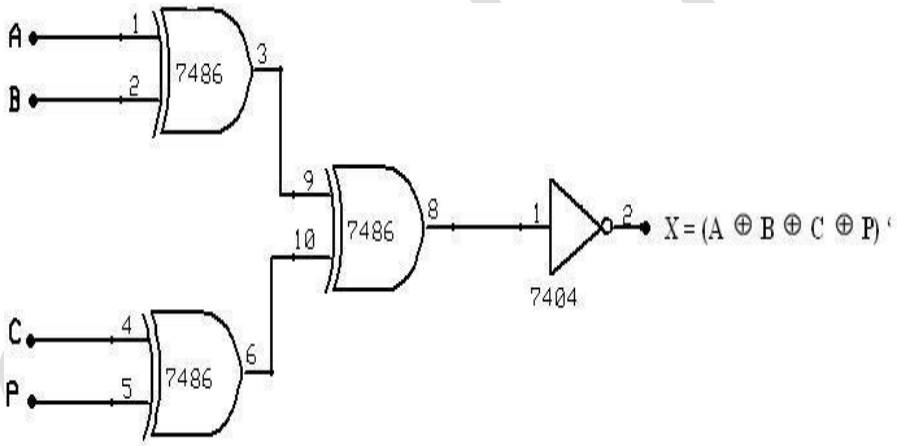
$$P = A'B'C' + A'BC + AB'C + ABC' = (A \oplus B \oplus C)'$$

CIRCUIT DIAGRAM:

ODD PARITY GENERATOR



ODD PARITY CHECKER



TRUTH TABLE:

SL.NO.	INPUT (4 - Bit Message Received)				OUTPUT (Parity Error Check)
	A	B	C	P	X
1.	0	0	0	0	1
2.	0	0	0	1	0
3.	0	0	1	0	0
4.	0	0	1	1	1

5.	0	1	0	0	0
6.	0	1	0	1	1
7.	0	1	1	0	1
8.	0	1	1	1	0
9.	1	0	0	0	0
10.	1	0	0	1	1
11.	1	0	1	0	1
12.	1	0	1	1	0
13.	1	1	0	0	1
14.	1	1	0	1	0
15.	1	1	1	0	0
16.	1	1	1	1	1

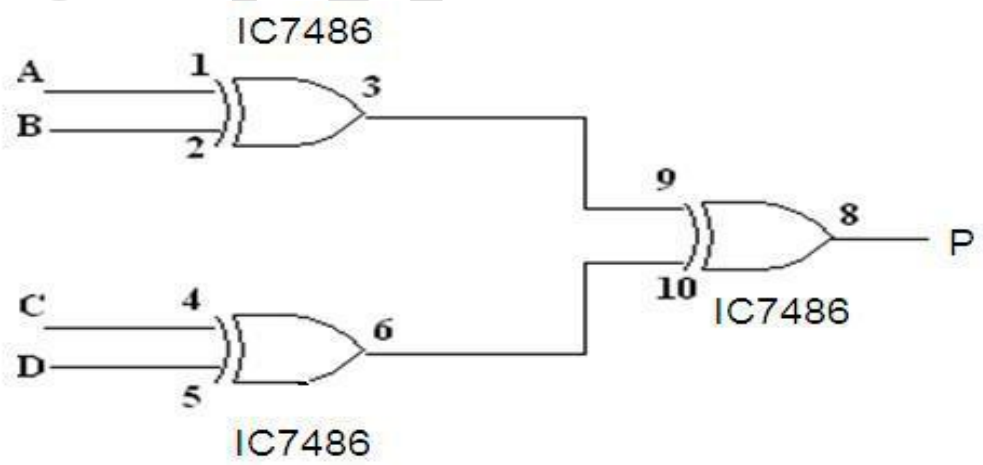
From the truth table the expression for the output parity checker bit is, $X(A, B, C, P) = \Sigma (0, 3, 5, 6, 9, 10, 12, 15)$

The above expression is reduced as,

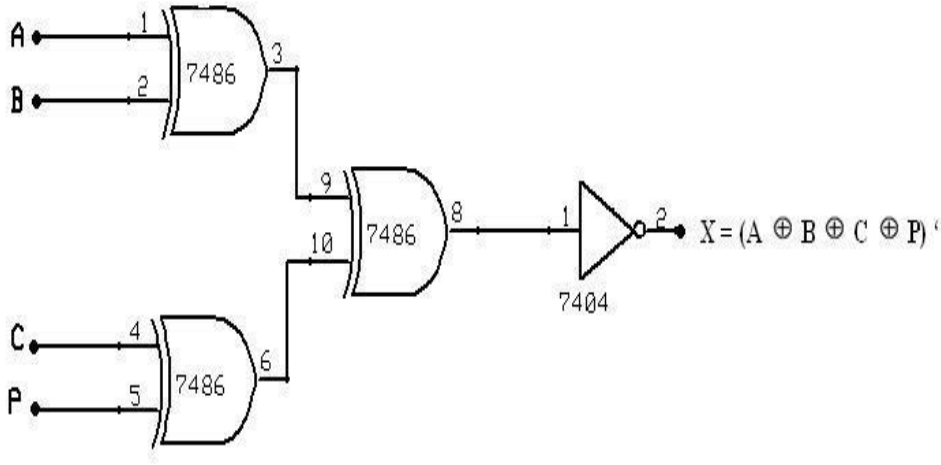
$X = (A \oplus B \oplus C \oplus P)$

EVENPARITYGENERATOR

CIRCUIT DIAGRAM:



PARITYCHECKER



PROCEDURE:

1. Connections are given as per the circuit diagrams.
2. For all the ICs 7th pin is grounded and 14th pin is given +5 V supply.
3. Apply the inputs and verify the truth table for the Parity generator and checker

POST LAB QUESTIONS:

1. How do parity generators help in error detection?
2. What happens if an extra bit is added to the data in a parity generator?
3. How do you detect errors using a parity checker circuit?
4. What is the main drawback of parity-based error detection?
5. Can a parity generator detect multiple-bit errors? Why or why not?

RESULT:

The design of the three bit odd Parity generator and checker& Even Parity generator and checker circuits was done and their truth tables were verified

CODE CONVERTER

Ex. No:3

Date:

AIM:

To construct and verify the performance of binary to gray and gray to binary.

APPARATUS REQUIRED:

S. No	Name	Specification	Quantity
1.	IC	7404, 7486,7408,7432	1
2.	Digital IC Trainer Kit		1
3.	Patch chords		As required

PRELAB QUESTIONS :

1. Why do we need code converters in digital circuits?
2. What are the different types of code converters?
3. How does a Binary to Gray code converter work?
4. What is the logic behind Gray to Binary conversion?
5. Why is Excess-3 a self-complementary code?

THEORY:

BINARY TO GRAY:

The MSB of the binary code alone remains unchanged in the Gray code. The remaining bits in the gray are obtained by EX-OR ing the corresponding gray code bit and previous bit in the binary code. The gray code is often used in digital systems because it has the advantage that only one bit in the numerical representation changes between successive numbers.

GRAY TO BINARY:

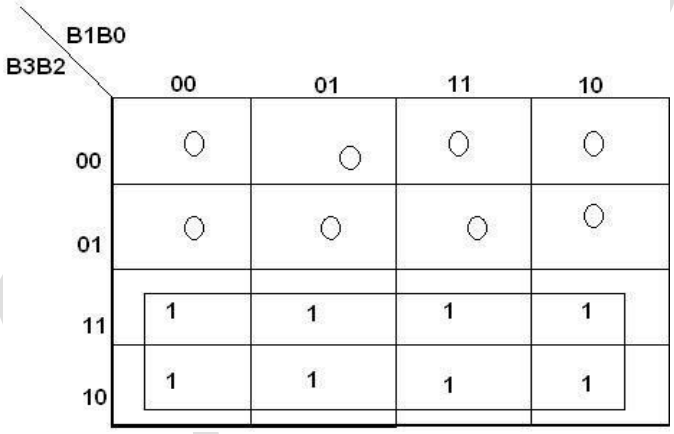
The MSB of the Gray code remains unchanged in the binary code the remaining bits are obtained by EX – OR ing the corresponding gray code bit and the previous output binary bit.

BINARY TO GRAY:

TRUTH TABLE

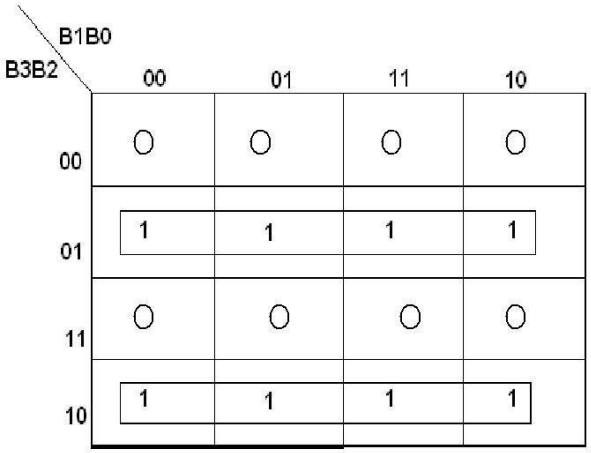
Decimal	Binary code				Gray code			
	D	C	B	A	D'	C'	B'	A'
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	1	0
5	0	1	0	1	0	1	1	1
6	0	1	1	0	0	1	0	1
7	0	1	1	1	0	1	0	0
8	1	0	0	0	1	1	0	0
9	1	0	0	1	1	1	0	1
10	1	0	1	0	1	1	1	1
11	1	0	1	1	1	1	1	0
12	1	1	0	0	1	0	1	0
13	1	1	0	1	1	0	1	1
14	1	1	1	0	1	0	0	1
15	1	1	1	1	1	0	0	0

K-Map for G_3



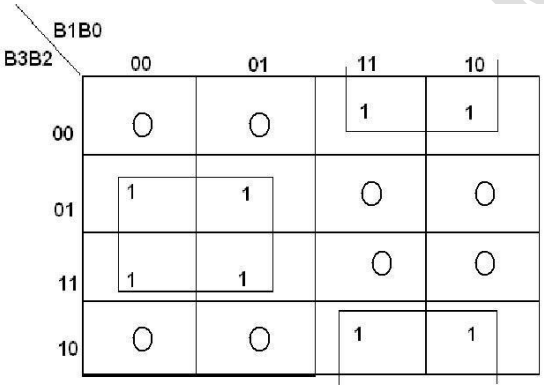
G3 = B3

K-Map for G_2



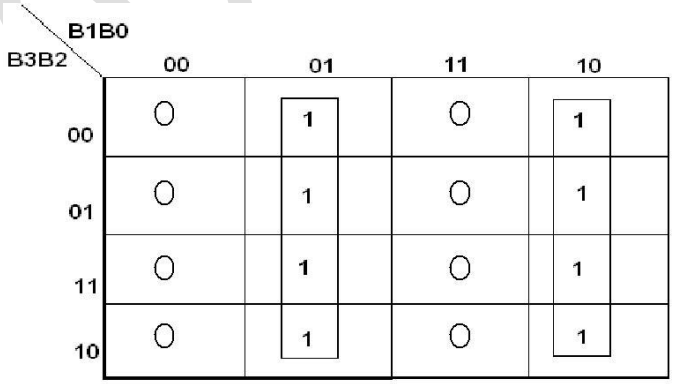
$G2 = B3 \oplus B2$

K-Map for G_1



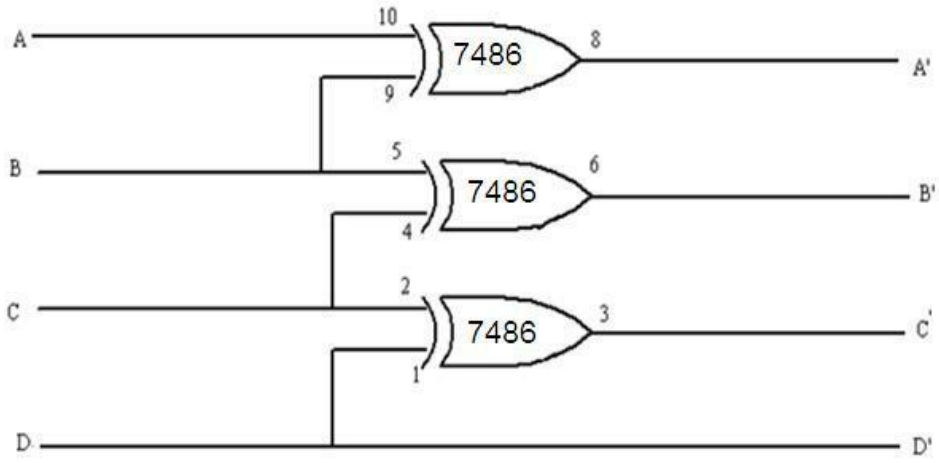
$G1 = B1 \oplus B2$

K-Map for G_0



$G0 = B1 \oplus B0$

Logic diagram :

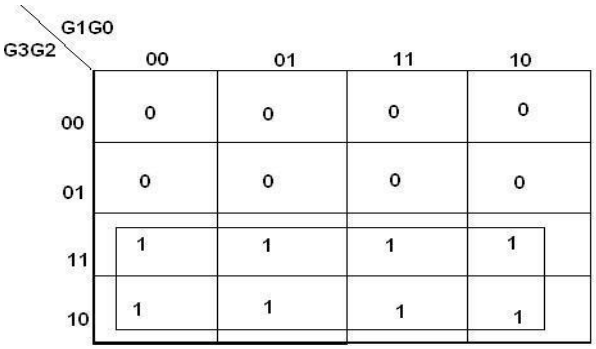


GRAY CODE TO BINARY CONVERTOR

TRUTH TABLE:

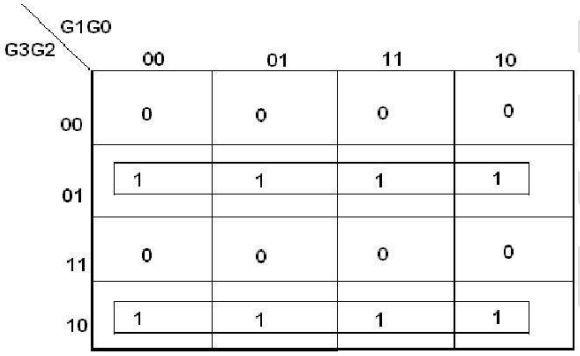
GRAY CODE				BINARY CODE			
G3	**G2**	**G1**	**G0**	**B3**	**B2**	**B1**	**B0**
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	1	0	0	1	0
0	0	1	0	0	0	1	1
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
0	1	0	1	0	1	1	0
0	1	0	0	0	1	1	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	1	1	0	1	0
1	1	1	0	1	0	1	1
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	0	0	1	1	1	1	0
1	0	0	0	1	1	1	1

K-Map for B3:



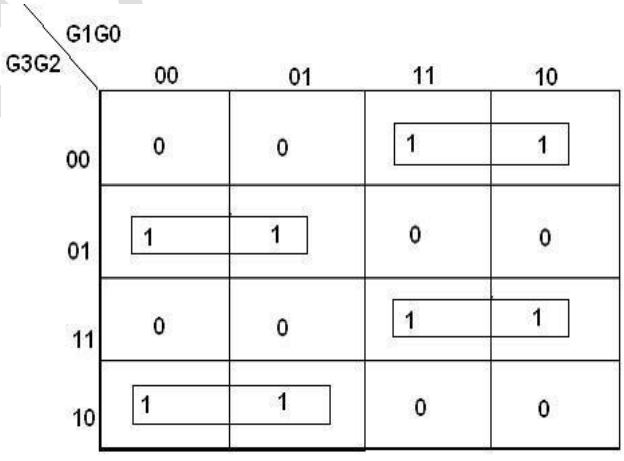
B3 = G3

K-Map for B2:



B2 = G3⊕G2

K-Map for B1:



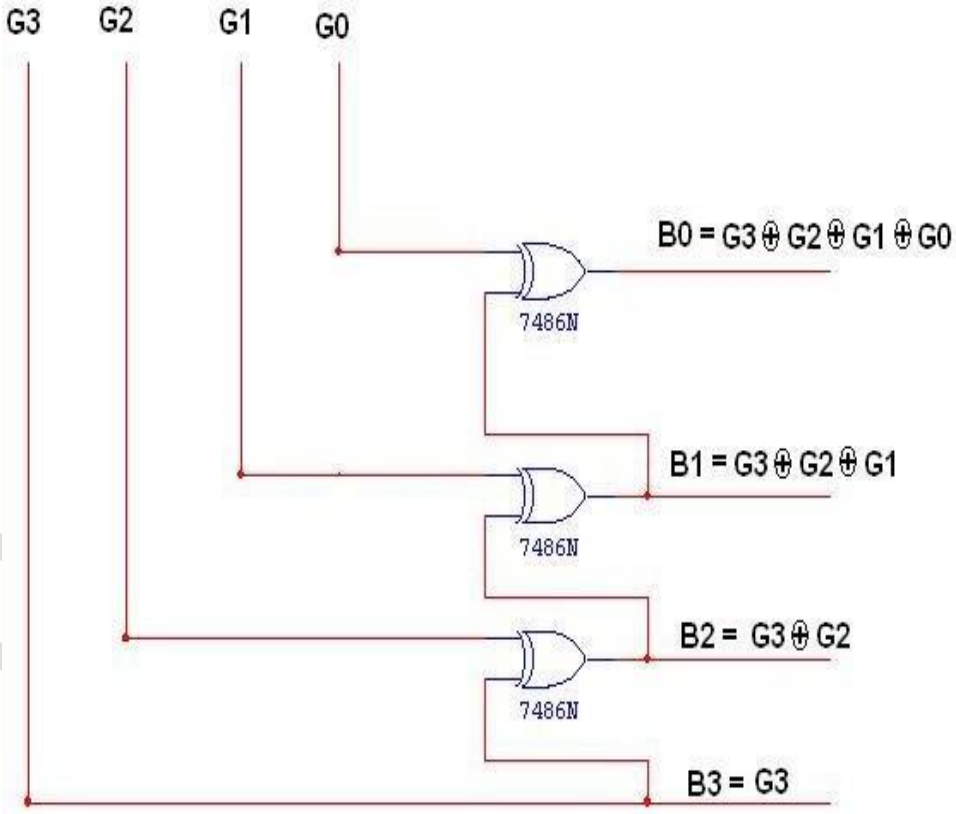
B1 = G3⊕G2⊕G1

K-Map for B0:

G3G2 \ G1G0	00	01	11	10
00	0	①	0	①
01	①	0	①	0
11	0	①	0	①
10	①	0	①	0

$$B0 = G3 \oplus G2 \oplus G1 \oplus G0$$

LOGIC DIAGRAM:

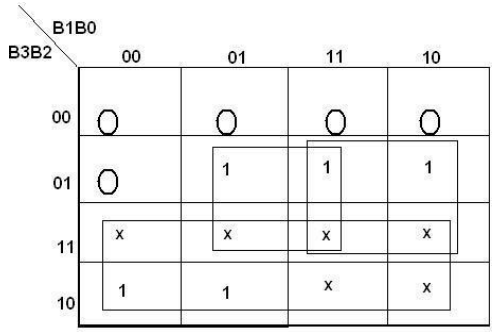


BCD TO EXCESS-3 CONVERTOR

TRUTH TABLE:

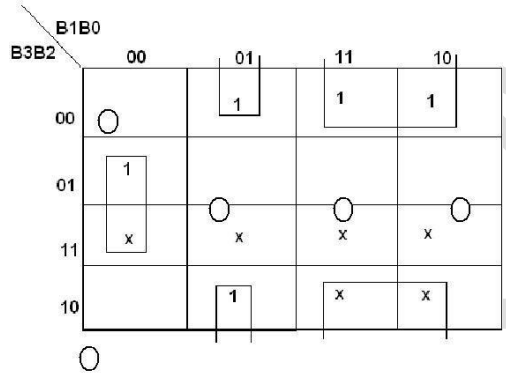
B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	x	x	x	x
1	0	1	1	x	x	x	x
1	1	0	0	x	x	x	x
1	1	0	1	x	x	x	x
1	1	1	0	x	x	x	x
1	1	1	1	x	x	x	X

K-Map for E3:



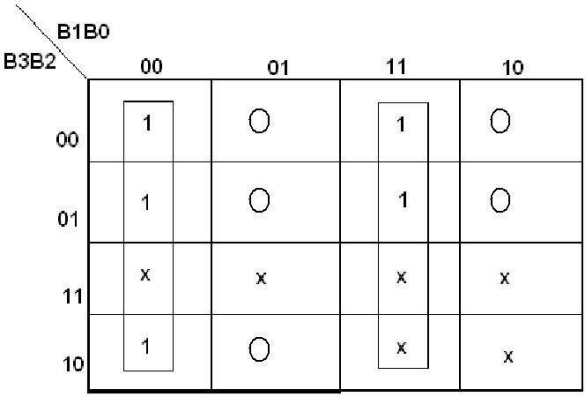
E3 = B3 + B2 (B0 + B1)

K-Map for E2:



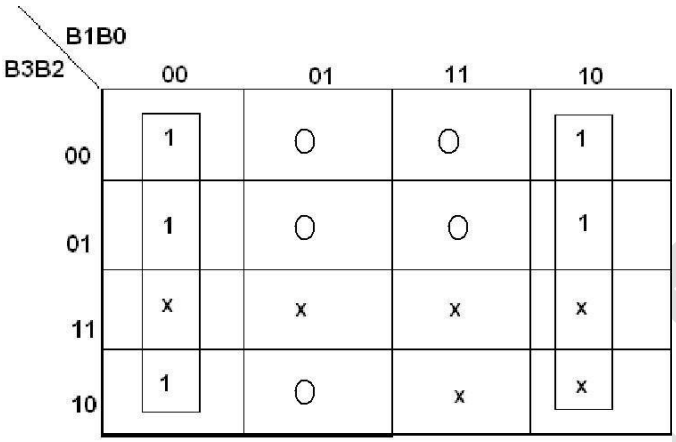
E2 = B2 ⊕ (B1 + B0)

K-Map for E1:



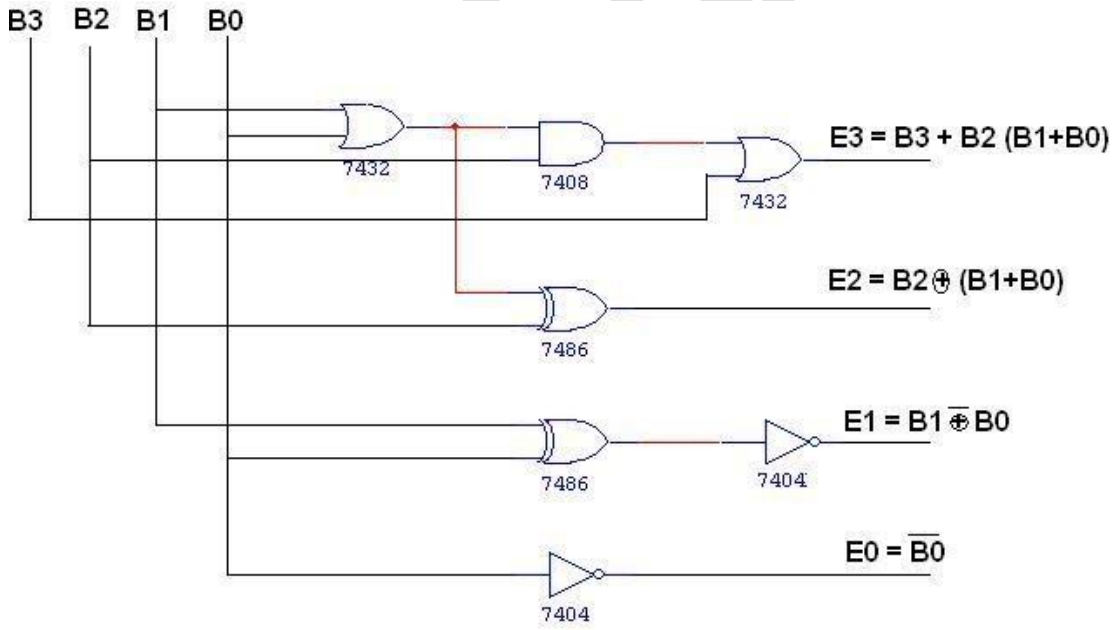
E1 = B1 $\bar{\oplus}$ B0

K-Map for E0:



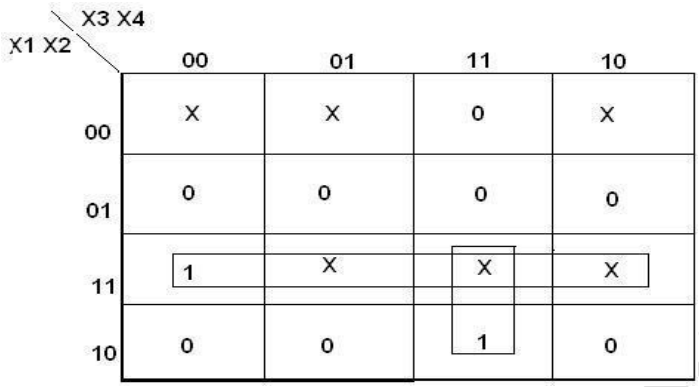
$E0 = \overline{B0}$

LOGIC DIAGRAM:



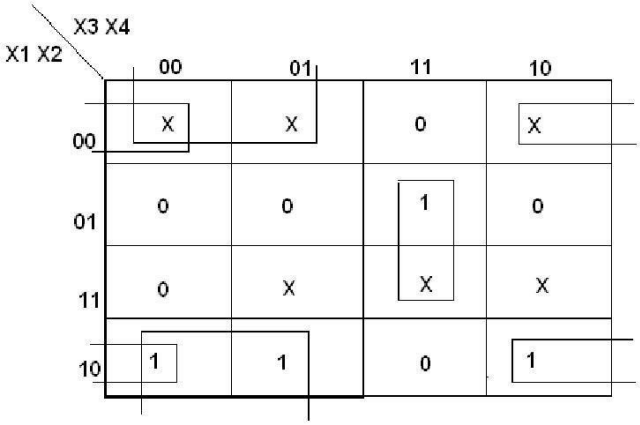
EXCESS-3 TO BCD CONVERTOR

K-Map for A:



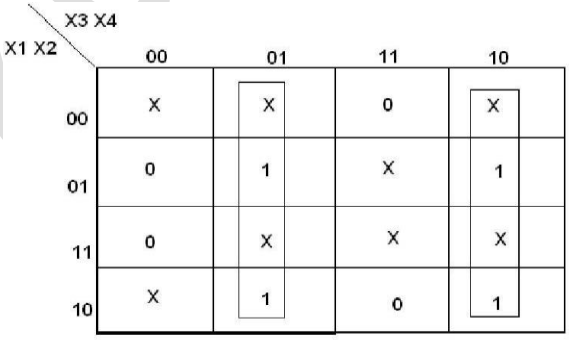
A = X1 X2 + X3 X4 X1

K-Map for B:



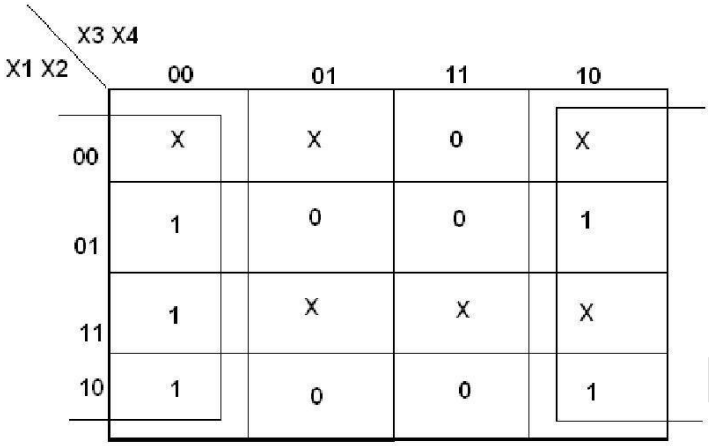
$$B = X2 \oplus (\overline{X3} + \overline{X4})$$

K-Map for C:



$$C = X3 \oplus X4$$

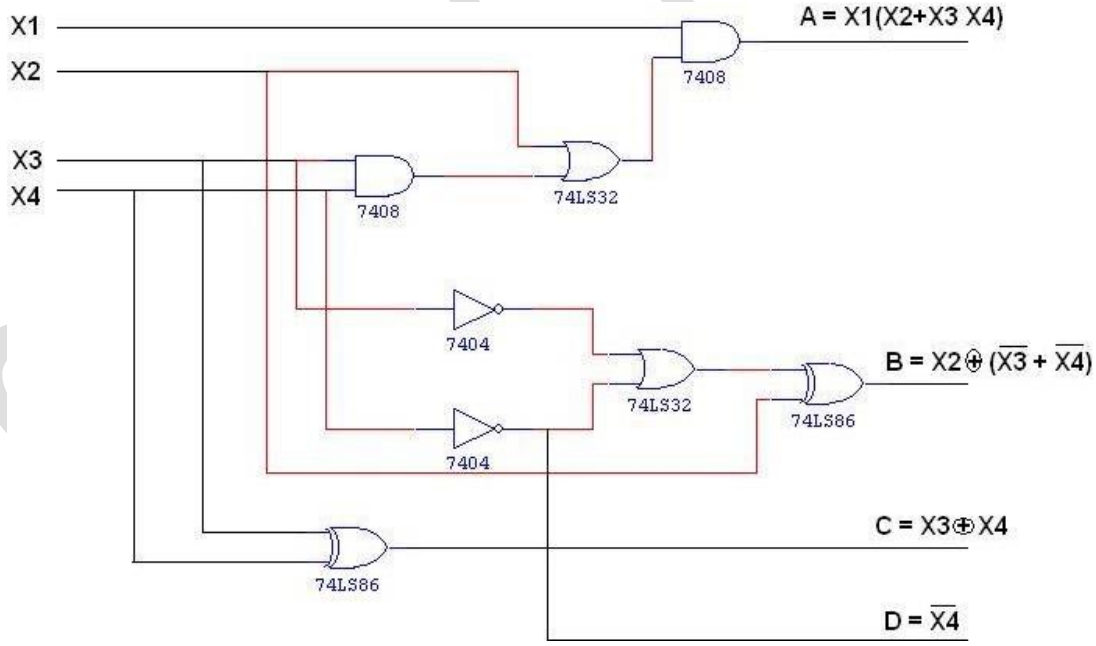
K-Map for D:



$D = \overline{X4}$

EXCESS-3 TO BCD CONVERTOR

LOGIC DIAGRAM:



PROCEDURE:

1. Connections are given as per the logic diagram
2. The given truth tables are verified.

POST LAB QUESTIONS :

1. How do you convert a binary number to Gray code**?**
2. What is the main advantage of using Gray code in encoders**?**
3. How many bits change when transitioning between two consecutive Gray code numbers?
4. What is the relation between Gray code and Karnaugh Maps (K-Maps)?
5. How does Gray code help in reducing glitches in digital circuits**?**

RESULT:

The design of the three bit Binary to Gray code converter & Gray to Binary code converter circuits was done and its truth table was verified

Ex. No: 4(a) **ENCODER**

Date:

AIM:

To design and implement encoder using IC 7432 (8-3 encoder)

APPARATUS REQUIRED:

S. No	Name	Specification	Quantity
1.	IC	7410	1
2.	Digital IC Trainer Kit		1
3.	Patch chords		-

PRE LAB QUESTIONS:

1. What is an encoder in digital electronics?
2. How many input and output lines does a 8-to-3 encoder have?
3. What is the general formula to determine the number of output lines for an encoder?
4. What is the difference between a combinational encoder and a sequential encoder?
5. How does an encoder differ from a decoder?

THEORY:

An encoder is digital circuit that has 2^n input lines and n output lines. The output lines generate a binary code corresponding to the input values 8 – 3 encoder circuit has 8 inputs, one for each of the octal digits and three outputs that generate the corresponding binary number. Enable inputs E_1 should be connected to ground and E_o should be connected to V_{CC}

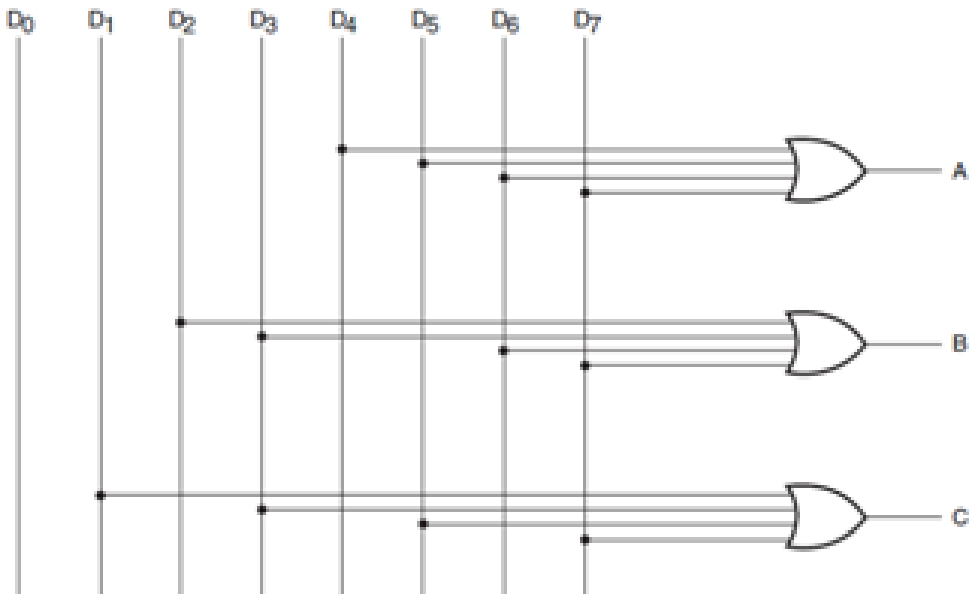
PROCEDURE:

1. Connections are given as per the logic diagram.
2. The truth table is verified by varying the inputs.

TRUTH TABLE

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	A	B	C
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	-0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

LOGIC DIAGRAM



POST LAB QUESTIONS:

1. What is the advantage of digital encoding over analog encoding?
2. What are the truth table and logic expressions for an 8-to-3 encoder?
3. How does an encoder handle multiple active inputs?
4. How can you detect errors in an encoder circuit?
5. What is the significance of the enable pin in an encoder?

RESULT:

Thus the design and implementation of encoder is done successfully

Ex.no: 4(b) **DECODER**

Date:

AIM:

To design and implement decoder using IC 7410 (3-8 decoder).

APPARATUS REQUIRED:

S. No	Name	Specification	Quantity
1.	IC	7410	1
2.	Digital IC Trainer Kit		1
3.	Patch chords		-

PRELAB QUESTIONS:

1. What is a decoder?
2. How many input and output lines does a 3-to-8 decoder have?
3. What is the truth table of a 3-to-8 decoder?
4. How does a decoder differ from an encoder?
5. What are the possible input values for a 3-to-8 decoder?

THEORY:

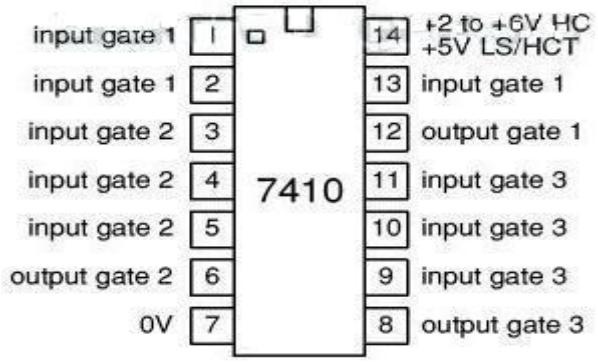
A decoder is a combinational circuit that converts binary information from n input lines to 2^n unique output lines.

In 3-8 line decoder the three inputs are decoded into right outputs in which each output representing one of the minterm of 3 input variables. IC 74155 can be connected as a dual 2*4 decoder or a single 3*8 decoder desired input in C_1 and C_2 must be connected together and used as the C input. G_1 and G_2 should be connected and used as the G (enable) input. G is the enable input and must be equal to 0 for proper operation.

PROCEDURE:

1. Connections are given as per the logic diagram.
2. The truth table is verified by varying the inputs.

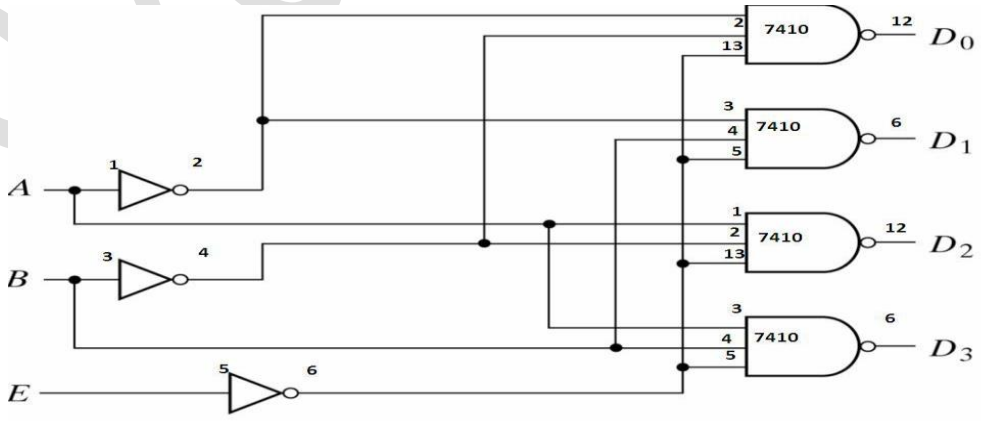
PIN DIAGRAM



TRUTH TABLE

E	A	B	D_0	D_1	D_2	D_3
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

LOGIC DIAGRAM



POST LAB QUESTIONS:

1. Why is a decoder called a demultiplexer (DEMUX) without data input**?**
2. What is the significance of a decoder in instruction decoding**?**
3. What type of logic gates are used to design a 3-to-8 decoder**?**
4. What will be the output if the input is 101**?**
5. What modifications are needed to make a 4-to-16 decoder using 3-to-8 decoders**?**

RESULT:

Thus the decoder circuit is designed and implemented

ASYNCHRONOUS COUNTER

Ex. No:5(a)

Date:

AIM:

To implement and verify the truth table of an asynchronous decade counter.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Digital IC trainer kit		1
2.	JK Flip Flop	IC 7476	2
4.	NAND gate	IC 7408	1
5.	Connecting wires		As required

PRELAB QUESTIONS :

1. What is an asynchronous counter?
2. How does an asynchronous counter differ from a synchronous counter?
3. Why is an asynchronous counter called a ripple counter?
4. How does an up counter work in an asynchronous system?
5. How many flip-flops are required for a 4-bit asynchronous counter?

THEORY:

Asynchronous decade counter is also called as ripple counter. In a ripple counter the flip flop output transition serves as a source for triggering other flip flops. In other words the clock pulse inputs of all the flip flops are triggered not by the incoming pulses but rather by the transition that occurs in other flip flops. The term asynchronous refers to the events that do not occur at the same time. With respect to the counter operation, asynchronous means that the flip flop within the counter are not made to change states at exactly the same time, they do not because the clock pulses are not connected directly to the clock input of each flip flop in the counter.

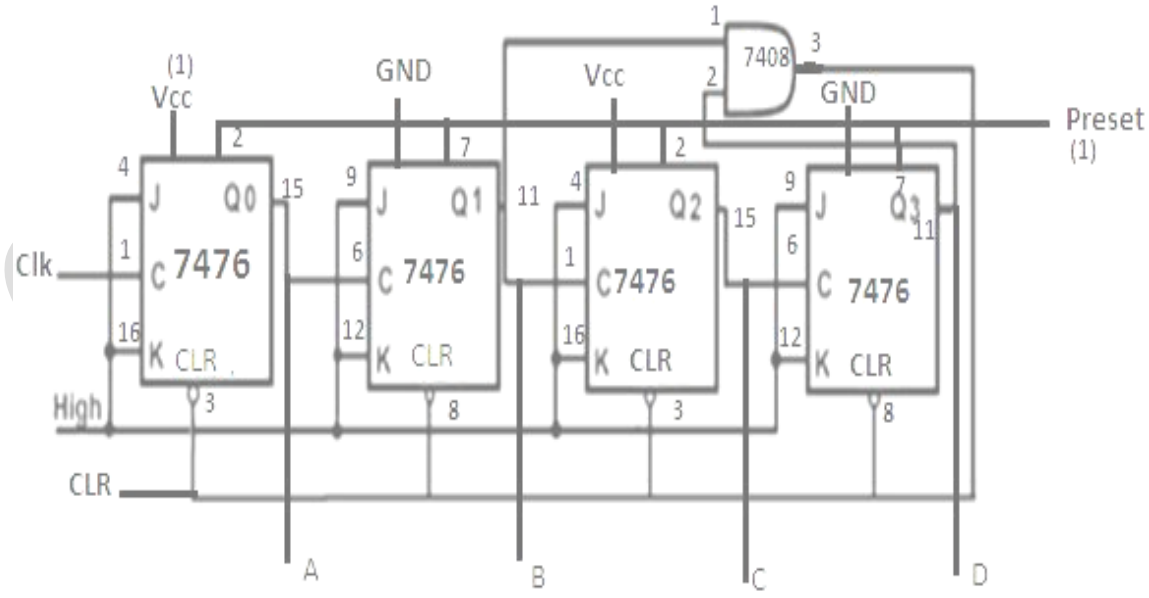
PROCEDURE:

1. Connections are given as per the circuit diagrams.
2. Apply the input and verify the truth table of the counter.

TRUTH TABLE:

S.No	CLOCK PULSE	OUTPUT			
		D(MSB)	C	B	A(LSB)
1	0	0	0	0	0
2	1	0	0	0	1
3	2	0	0	1	0
4	3	0	0	1	1
5	4	0	1	0	0
6	5	0	1	0	1
7	6	0	1	1	0
8	7	0	1	1	1
9	8	1	0	0	0
10	9	1	0	0	1
11	10	0	0	0	0

CIRCUIT DIAGRAM:



POST LAB QUESTIONS :

1. How does the clock signal propagate in an asynchronous counter?
2. What is the working principle of an asynchronous counter?
3. What are the main components of an asynchronous counter?
4. Why is an asynchronous counter not suitable for high-speed applications?
5. How many states does a 4-bit asynchronous counter have?

RESULT :

Thus the implementation and verification of the truth table of an asynchronous decade counter is done successfully.

SYNCHRONOUS COUNTER

Ex. No:5(b)

Date:

AIM:

To design and implement 4-bit synchronous BCD counter.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Digital IC trainer kit		1
2.	JK Flip Flop	IC7476	2
3.	AND gate	IC7408	2
4.	OR gate	IC7432	1
5	Connecting wires		As required

PRELAB QUESTIONS:

1. What is a synchronous counter?
2. What are the advantages of a synchronous counter?
3. What are the types of synchronous counters?
4. What is the role of flip-flops in a synchronous counter?
5. Where are synchronous counters used in digital electronics?

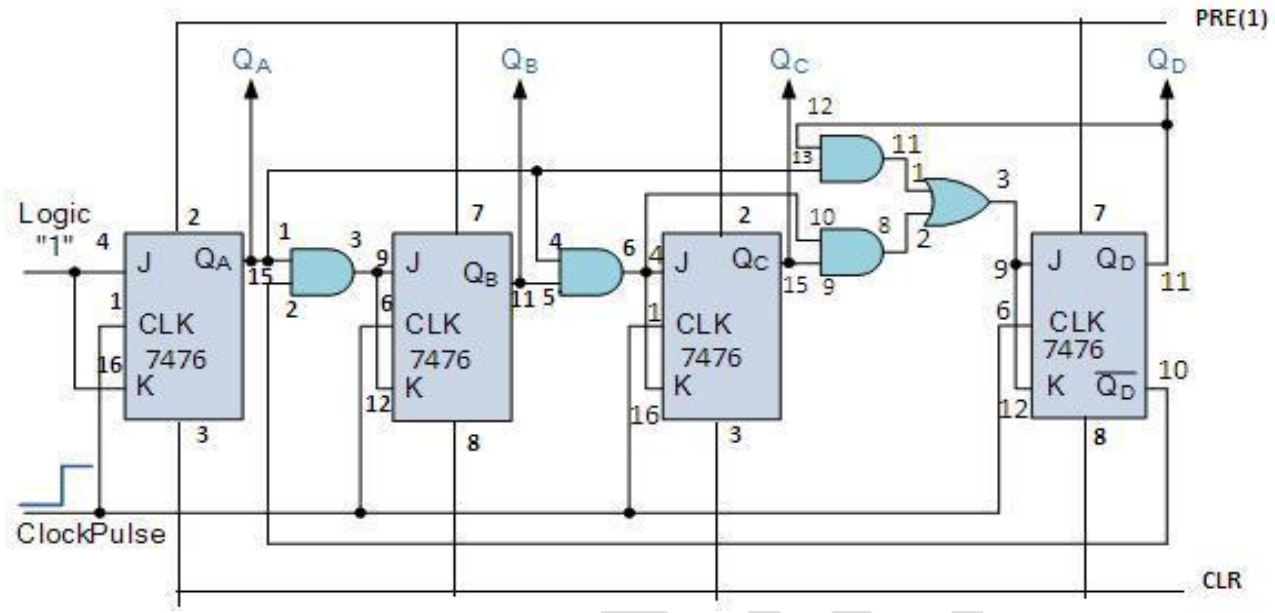
THEORY:

A counter is a register capable of counting number of clock pulse arriving at the clock input. In synchronous counter all the flip-flops are clocked simultaneously .It is faster in speed because of the propagation delay of the single flip-flop is involved. It is also called as a parallel counter. A BCD synchronous counter can be called as a decade counter or mod-10 counter. It requires 4 flip flops ($10<=2^4$). So there are 16 possible states out of which 10 are valid and other 6 are invalid.

PROCEDURE:

1. Connections are given as per the circuit diagrams.
2. Apply the input and verify the truth table of the counter

CIRCUIT DIAGRAM:



TRUTH TABLE:

Present State				Next State				Excitation Required							
Q_4	Q_3	Q_2	Q_1	Q_4	Q_3	Q_2	Q_1	J_4	K_4	J_3	K_3	J_2	K_2	J_1	K_1
0	0	0	0	0	0	0	1	0	X	0	X	0	X	1	X
0	0	0	1	0	0	1	0	0	X	0	X	1	X	X	1
0	0	1	0	0	0	1	1	0	X	0	X	X	0	1	X
0	0	1	1	0	1	0	0	0	X	1	X	X	1	X	1
0	1	0	0	0	1	0	1	0	X	X	0	0	X	1	X
0	1	0	1	0	1	1	0	0	X	X	0	1	X	X	1
0	1	1	0	0	1	1	1	0	X	X	0	X	0	1	X
0	1	1	1	1	0	0	0	1	X	X	1	X	1	X	1
1	0	0	0	1	0	0	1	X	0	0	X	0	X	1	X
1	0	0	1	0	0	0	0	X	1	0	X	0	X	X	1

POST LAB QUESTIONS:

1. What would happen if the clock signals to different flip-flops in a synchronous counter were not properly synchronized?
2. What are common issues faced while designing a synchronous counter in hardware?
3. How does a synchronous counter eliminate propagation delay?
4. What is the function of a clock in a synchronous counter?
5. What logic function is required to enable the toggling of each flip-flop in a synchronous counter?

RESULT:

Thus the synchronous counter circuits were designed and the outputs were verified.

Ex. No:6 **SHIFT REGISTERS**

Date:

AIM:

To implement the following shift register using flip flop

(i) SIPO

(ii) SISO

(iii) PISO

(iv) PIPO

APPARATUS REQUIRED:

S. No	Name	Specification	Quantity
1.	IC	7474	1
2.	Digital IC Trainer Kit		1
3.	Patch chords		-

PRELAB QUESTIONS:

1. What is a shift register?
2. What are the types of shift registers?
3. What is the function of a shift register?
4. How many flip-flops are required to store 8 bits of data?
5. What type of flip-flop is commonly used in shift registers?

THEORY:

A register is used to move digital data. A shift register is a memory in which information is shifted from one position in to another position at a line when one clock pulse is applied. The data can be shifted either left or right direction towards right or towards left.

A shift register can be used in four ways depending upon the input in which the data are entered in to and takes out of it. The four configuration are given as

Serial input – Serial output

Parallel input – Serial output

Serial input – Parallel output

Parallel input – Parallel output

RS or JK flip flop are used to construct shift register have D flip flop is used for constructing shift register.

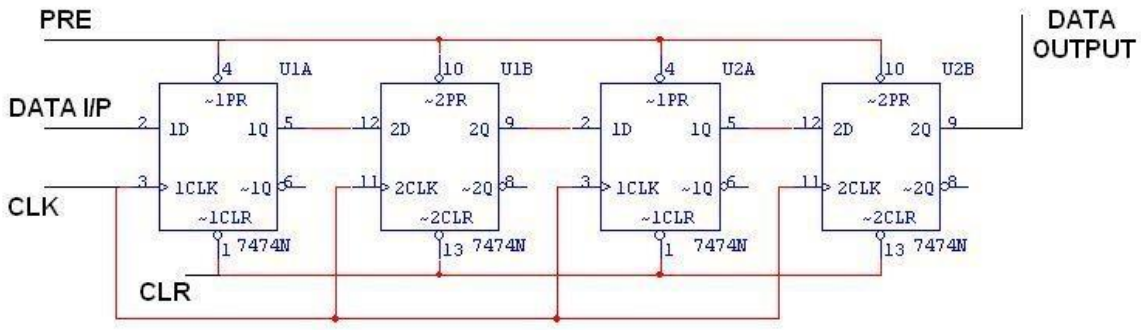
1. Serial-in to Parallel-out (SIPO) - the register is loaded with serial data, one bit at a time, with the stored data being available at the output in parallel form.
2. Serial-in to Serial-out (SISO) - the data is shifted serially "IN" and "OUT" of the register, one bit at a time in either a left or right direction under clock control.
3. Parallel-in to Serial-out (PISO) - the parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.
4. Parallel-in to Parallel-out (PIPO) - the parallel data is loaded simultaneously into the register, and transferred together to their respective outputs by the same clock pulse.

PROCEDURE:

1. Give the connections as per the circuit
2. Set or Reset at the pin 2 which it's the MSB of serial data.
3. Apply a single clock Set or Reset second digital input at pin 2.
4. Repeat step 2 until all 4-bit data are taken away.

SISO

LOGIC DIAGRAM:

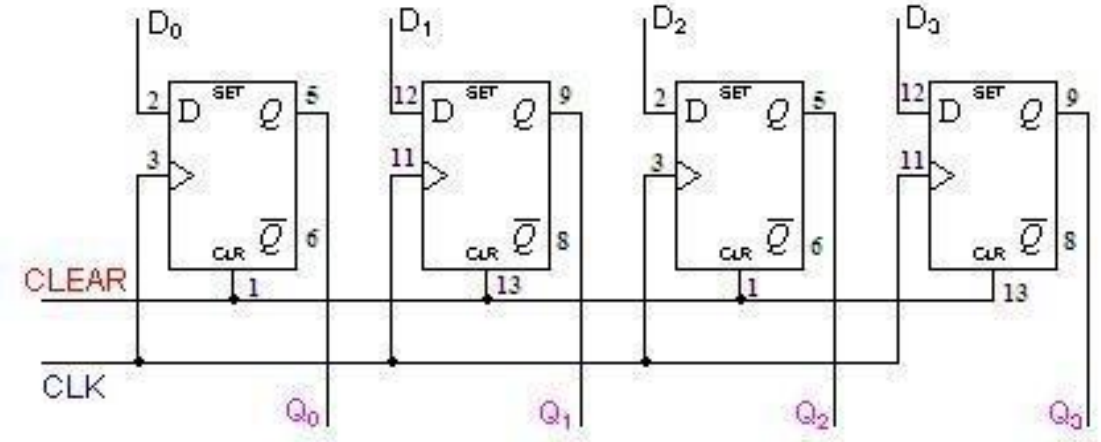


TRUTH TABLE:

CLK	Serial In	Serial Out
1	1	0
2	0	0
3	0	0
4	1	1
5	X	0
6	X	0
7	X	1

SIPO

LOGIC DIAGRAM



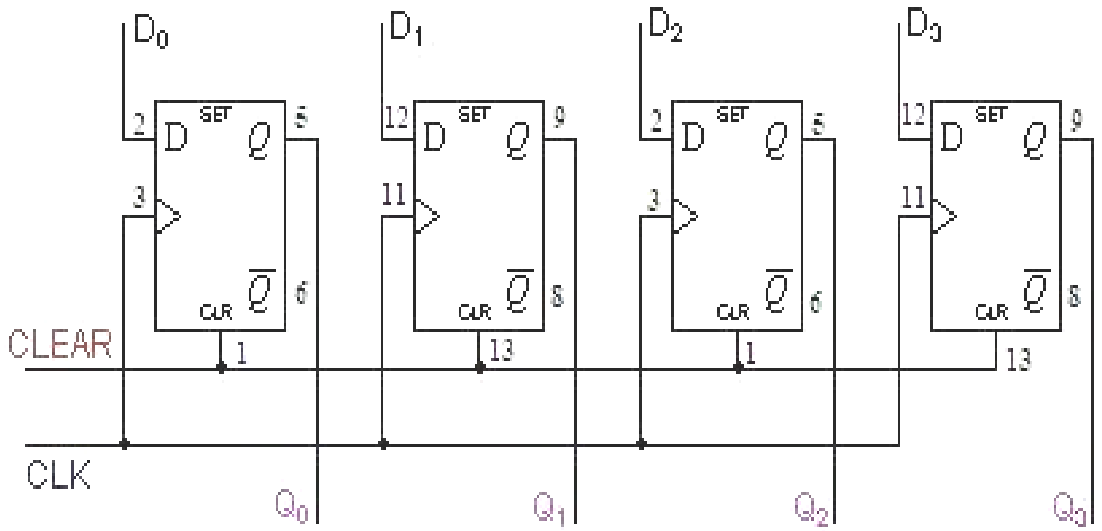
TRUTH TABLE

No of clk pulse	Serial input D_{in}	Parallel output			
		Q3	Q2	Q1	Q0
0	0	0	0	0	0
1	1	0	0	0	1
2	1	0	0	1	1
3	0	0	1	1	0
4	1	1	1	0	1
5	0	1	0	1	0

6	0	0	1	0	0
7	0	1	0	0	0
8	0	0	0	0	0

PIPO

LOGIC DIAGRAM

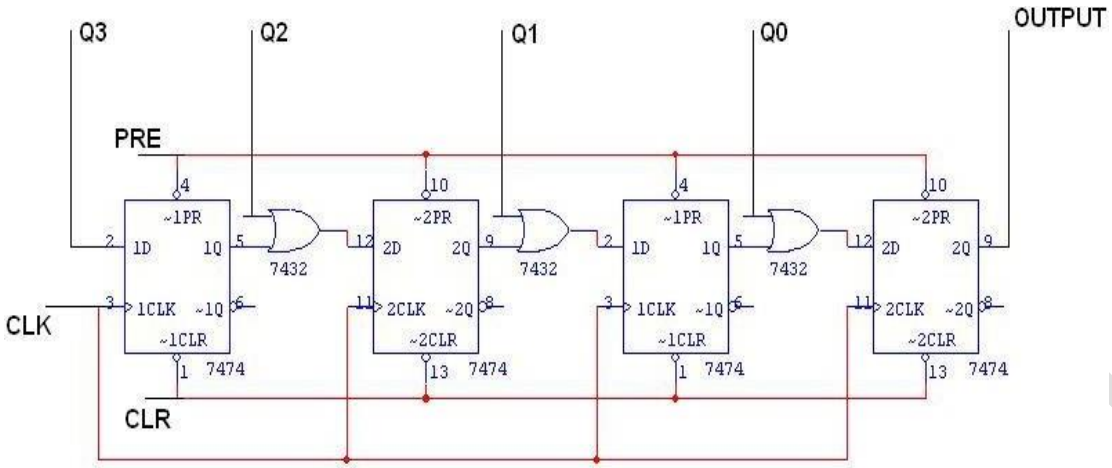


TRUTH TABLE

Clock	Parallel input				Parallel output			
	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0	0	0	0	0
1	1	1	0	1	1	1	0	1

PISO :

LOGIC DIAGRAM:



TRUTH TABLE:

CLK	Q3	Q2	Q1	Q0	O/P
0	1	0	0	1	1
1	0	0	0	0	0
2	0	0	0	0	0
3	0	0	0	0	1

POST LAB QUESTIONS:

1. What is the significance of the 'shift enable' signal in a shift register?
2. Where are shift registers used in real-world applications?
3. Why is a shift register used in UART communication?
4. Why is a shift register called a sequential circuit?
5. How do we determine the number of clock pulses required to shift out data in a shift register?

RESULT:

Thus the SISO, SIPO, PISO, PIPO shift registers were designed and implemented

Ex. No: 7 **MULTIPLEXER & DEMULTIPLEXER**

Date:

AIM:

To study the truth table of a 4X1 Multiplexer & 1X4 Demultiplexer.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Digital IC trainer kit		1
2.	OR gate	IC 7432	
3.	NOT gate	IC 7404	
4.	AND gate (three input)	IC 7411	
5.	Connecting wires		As required

PRELAB QUESTIONS:

1. What is a multiplexer (MUX)?
2. What is a Demultiplexer (DEMUX)?
3. How does a DEMUX differ from a MUX?
4. How many select lines are required for an 1 to 4 MUX?
5. How many select lines are required for an 4 to 1 DEMUX?

THEORY:

Multiplexer is a digital switch which allows digital information from several sources to be routed onto a single output line. The basic multiplexer has several data input lines and a single output line. The selection of a particular input line is controlled by a set of selection lines. Normally, there are 2^n input lines and n selector lines whose bit combinations determine which input is selected. Therefore, multiplexer is 'many into one' and it provides the digital equivalent of an analog selector switch.

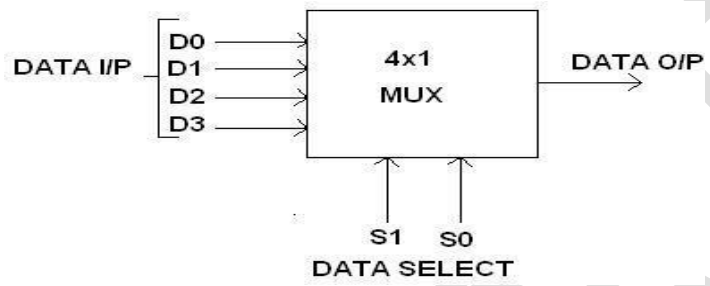
A Demultiplexer is a circuit that receives information on a single line and transmits this information on one of 2^n possible output lines. The selection of specific output line is controlled by the values of n selection lines.

PROCEDURE:

1. Connections are given as per the circuit diagrams.
2. For all the ICs 7^{th} pin is grounded and 14^{th} pin is given +5 V supply.
3. Apply the inputs and verify the truth table for the multiplexer & demultiplexer.

4:1 MULTIPLEXER

BLOCK DIAGRAM FOR 4:1 MULTIPLEXER:



FUNCTION TABLE:

S1	S0	INPUTS Y
0	0	D0 → D0 S1' S0'
0	1	D1 → D1 S1' S0
1	0	D2 → D2 S1 S0'
1	1	D3 → D3 S1 S0

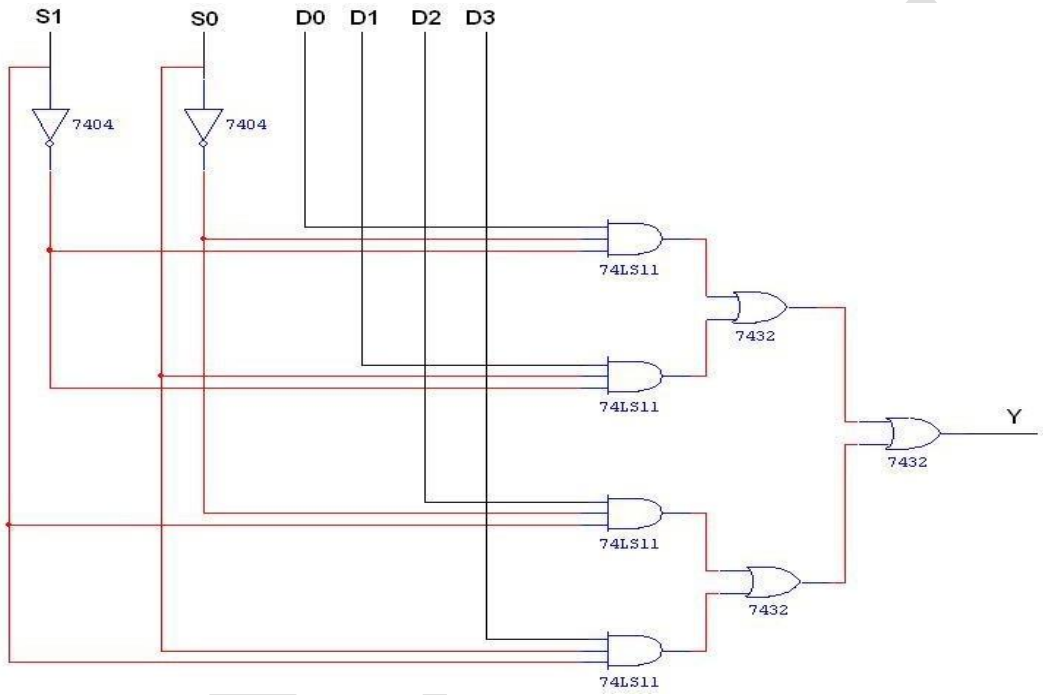
Y = D0 S1' S0' + D1 S1' S0 + D2 S1 S0' + D3 S1 S0

TRUTH TABLE:

X	Y	OUTPUTS (Y)
0	**0**	**D0 → D0 X' Y'**
0	**1**	**D1 → D1 X' Y**

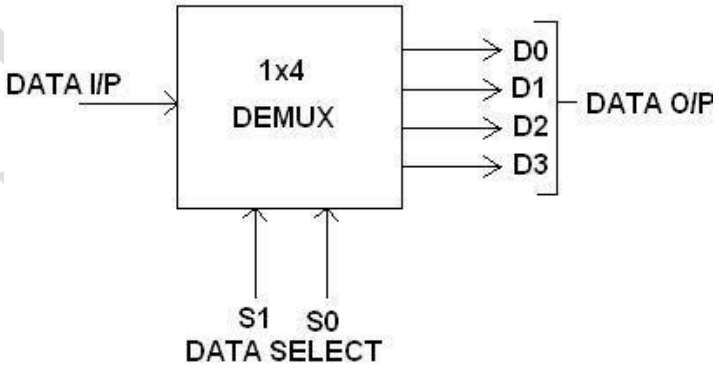
1	**0**	**D2 → D2 X Y'**
1	**1**	**D3 → D3 X Y**

LOGIC DIAGRAM FOR MULTIPLEXER:



1:4 DEMULTIPLEXER

BLOCK DIAGRAM FOR 1:4 DEMULTIPLEXER:



FUNCTION TABLE:

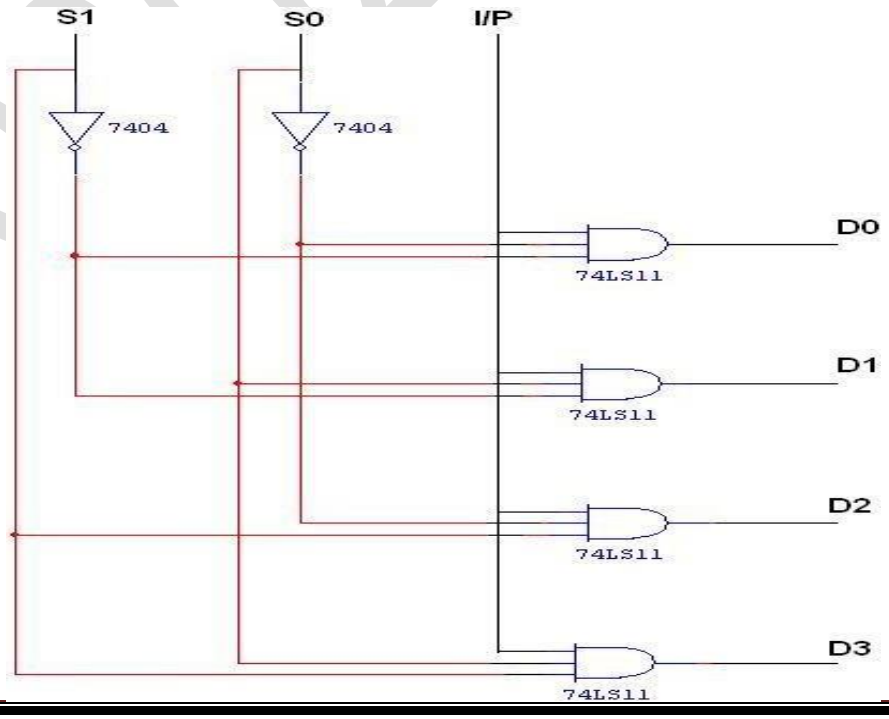
S1	S0	INPUT
0	0	X → D0 = X S1' S0'
0	1	X → D1 = X S1' S0
1	0	X → D2 = X S1 S0'
1	1	X → D3 = X S1 S0

Y = X S1' S0' + X S1' S0 + X S1 S0' + X S1 S0

TRUTH TABLE:

INPUT			OUTPUT			
S1	**S0**	**I/P**	**D0**	**D1**	**D2**	**D3**
0	0	0	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	1	0	1	0	0
1	0	0	0	0	0	0
1	0	1	0	0	1	0
1	1	0	0	0	0	0
1	1	1	0	0	0	1

LOGIC DIAGRAM FOR DEMULTIPLEXER:



POST LAB QUESTIONS :

1. What is the role of the enable signal in a DEMUX?
2. What is the Boolean equation for a 1-to-4 DEMUX?
3. Why is a DEMUX called a “data distributor”?
4. Why is a MUX called a “data Selector”?
5. What is the function of the select lines in a MUX & DEMUX?

RESULT:

The design of the 4x1 Multiplexer and 1x4 Demultiplexer circuits was done and their truth tables were verified

TIMER IC
APPLICATIONS - I

Ex. No:8(a)
Date:

(ASTABLMULTIVIBRATOR)

AIM:

To design an astable multivibrator circuit for the given specifications using 555 Timer IC.

APPARATUS REQUIRED:

S. No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Timer IC	IC 555	1
5.	Bread Board		1
6.	Resistors		As required
7.	Capacitors		As required
8.	Connecting wires and probes		As required

PRELAB QUESTIONS:

1. What is an astable multivibrator?
2. Which Timer IC is commonly used for astable multivibrator applications?
3. Why is an astable multivibrator called ‘free-running’?
4. What are the components required to design a 555 Timer-based astable multivibrator?
5. What is the function of resistors R1 and R2 in the astable mode?

THEORY:

An astable multivibrator, often called a free-running multivibrator, is a rectangular-wave-generating circuit. This circuit do not require an external trigger to change the state of the output. The time during which the output is either high or low is determined by two resistors and a capacitor, which are connected externally to the 555 timer. The time during which the capacitor charges from 1/3 V_{cc} to 2/3 V_{cc} is equal to the time the output is high and is given by,

$$t_c = 0.69 (R_1 + R_2) C$$

Similarly the time during which the capacitor discharges fro

m 2/3 V_{cc} to 1/3 V_{cc} is equal to the time the output is low and is given by,

$$t_d = 0.69 (R_2) C$$

Thus the total time period of the output waveform is,

$$T = t_c + t_d = 0.69 (R_1 + 2 R_2) C$$

The term duty cycle is often used in conjunction with the astable multivibrator. The duty cycle is the ratio of the time t_c during which the output is

% duty cycle = $[R_2 / (R_1 + 2 R_2)] \times 100\%$ or $t_d / t_c \times 100\%$

DESIGN:

Given f= 11.11 KHz and duty cycle = 23% Therefore, Total time period, $T = 1/f = 90 \times 10^{-6}$ s

We know, duty cycle = t_d / T

$23 / 100 = t_d / 90 \times 10^{-6}$, $t_d = 0.23 \times 90 \times 10^{-6}$

Therefore, $t_d = 20.7 \times 10^{-6}$ s
and $t_c = T - t_d = 90 \times 10^{-6} - 20.7 \times 10^{-6} = 69.3 \times 10^{-6}$ s

We also know for an astable multivibrator $t_d = 0.69 (R_2) C$
Assume $C = 0.01 \times 10^{-6}$ F
$R_2 = t_d /(0.69 \times C) = 20.7 \times 10^{-6} / (0.69 \times 0.01 \times 10^{-6})$
Therefore, $R_2 = 3K\Omega$
$t_c = 0.69 (R_1 + R_2) C$

$R_1 = (t_c / (0.69 \times C)) - R_2$

$R_1 = (69.3 \times 10^{-6} / (0.69 \times 0.01 \times 10^{-6})) - 3000$

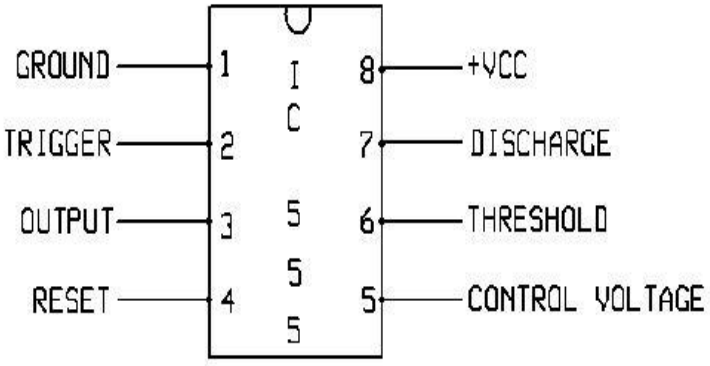
Therefore, $R_1 = 7\ K\Omega \approx 6.8\ K\Omega \approx 7.5\ K\Omega$

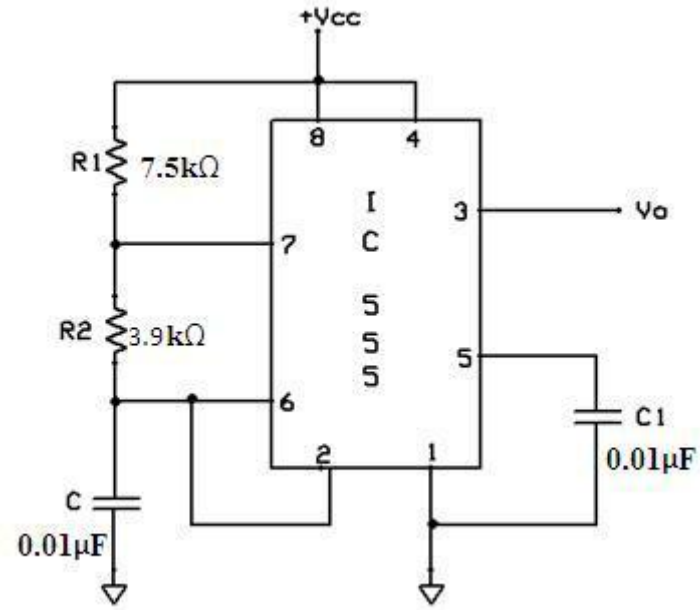
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. + 5V supply is given to the + V_{cc} terminal of the timer IC.
3. At pin 3 the output waveform is observed with the help of a CRO

4. At pin 6 the capacitor voltage is obtained in the CRO and the V_0 and V_c voltage waveforms are plotted in a graph sheet.

PIN DIAGRAM:



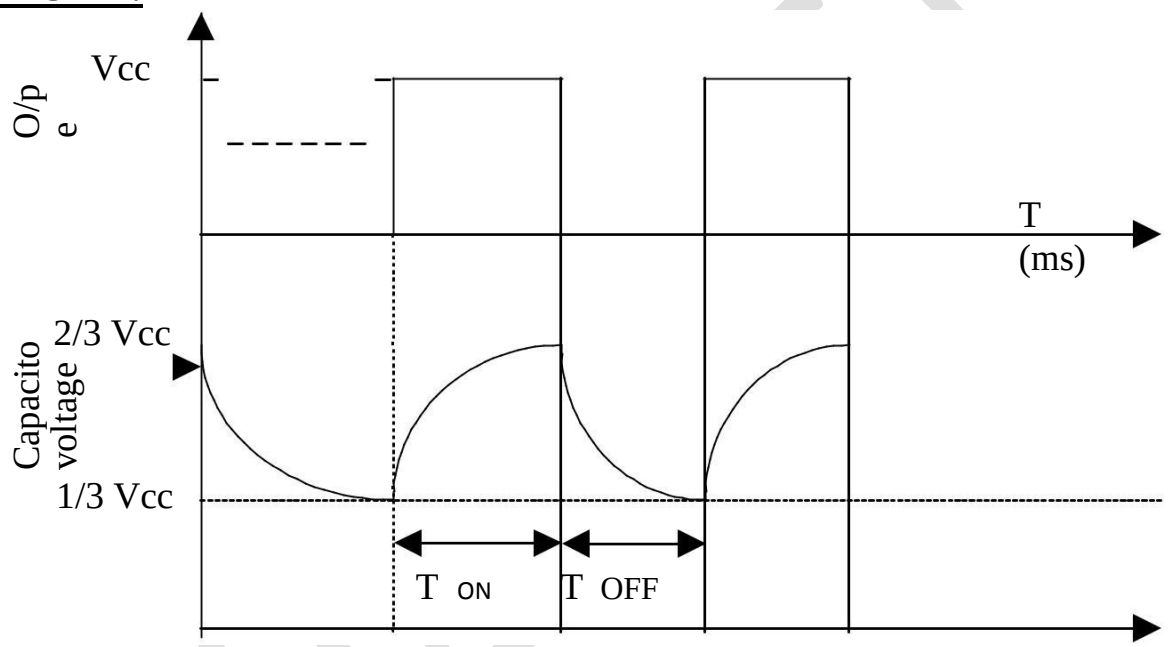


TABULATION:

WAVE FORM	AMPLITUDE (NUMBER OF DIVISIONS * VOLTAGES PER DIVISIONS)	TIME PERIOD(NUMBER OF DIVISIONS * TIME PER DIVISIONS)	
		t_c	t_d

OUT PUT VOLTAGE			
INPUT VOLTAGE			

WAVEFORM:



POST LAB QUESTIONS:

1. What is the role of pin 5 (Control Voltage) in a 555 Timer?
2. Where are astable multivibrators used in real life?
3. How can an astable multivibrator be used in a digital clock circuit?
4. What modifications are needed to convert an astable multivibrator into a monostable multivibrator?
5. How can a 555 Timer astable circuit be used for Pulse Width Modulation (PWM)?

RESULT:

The design of the Astable multivibrator circuit was done and the output voltage and capacitor voltage waveforms were obtained

Ex. No:8(b) **TIMER IC APPLICATIONS –II**
Date: **(MONOSTABLE MULTIVIBRATOR)**

AIM:

To design a monostable multivibrator for the given specifications using 555 Timer IC.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz, Analog	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Timer IC	IC 555	1
5.	Bread Board		1
6.	Resistors		As required
7.	Capacitors		As required

PRELAB QUESTIONS:

1. What is a monostable multivibrator?
2. Why is it called ‘monostable’?
3. What is the function of a 555 Timer IC in monostable mode?
4. What components are required to design a monostable multivibrator using a 555 Timer?
5. What is the formula for pulse width (time duration) in a monostable multivibrator?

THEORY:

A monostable multivibrator often called a one-shot multivibrator is a pulse generating circuit in which the duration of the pulse is determined by the RC network connected externally to the 555 timer. In a stable or stand-by state the output of the circuit is approximately zero or at logic low level. When an external trigger pulse is applied, the output is forced to go high (approx. V_{cc}). The time during which the output remains high is given by,

$$t_p = 1.1\ R_1\ C$$

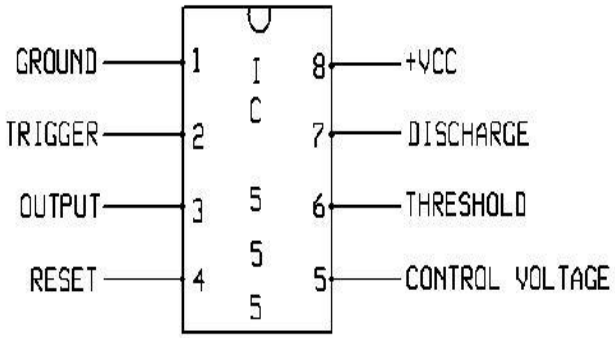
At the end of the timing interval, the output automatically reverts back to its logic low state. The output stays low until a trigger pulse is applied again. Then the cycle repeats.

Thus the monostable state has only one stable state hence the name monostable.

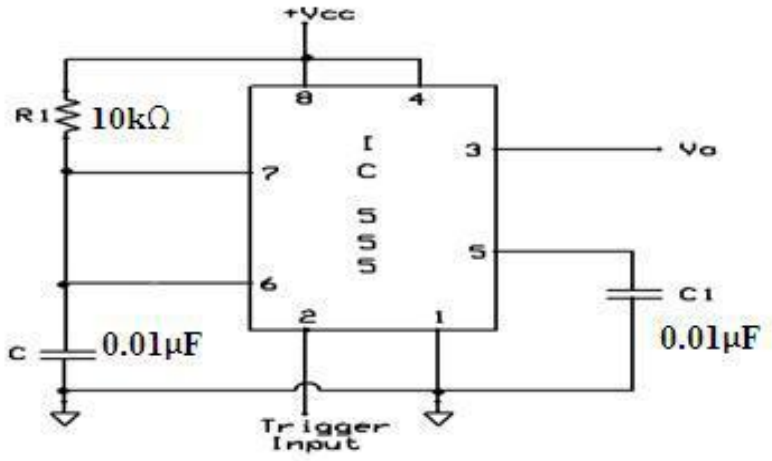
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. + 5V supply is given to the + V_{cc} terminal of the timer IC.
3. A negative trigger pulse of 5V, 2 KHz is applied to pin 2 of the 555 IC
   At pin 3 the output waveform is observed with the help of a CRO
4. At pin 3 the output waveform is observed with the help of a CRO
5. At pin 6 the capacitor voltage is obtained in the CRO and the V_0 and V_c voltage waveforms are plotted in a graph sheet.

PIN DIAGRAM:



CIRCUIT DIAGRAM OF MONOSTABLE MULTIVIBRATOR:



POST LAB QUESTIONS:

1. How does a monostable multivibrator differ from an astable multivibrator?
2. What is the purpose of the external trigger signal?
3. What happens if the trigger signal remains LOW for too long?
4. What modifications are required to use a 555 monostable circuit for long-duration timing?
5. What is the role of the discharge pin (Pin 7) in monostable mode?

RESULT:

The design of the monostable multivibrator circuit was done and the output voltage and capacitor voltage waveforms were obtained

Ex. No:9(a) **APPLICATIONS OF OP-AMP – I**
Date: **(INVERTING AND NON – INVERTING AMPLIFIER)**

a. INVERTING AMPLIFIER

AIM:

To design an Inverting Amplifier for the given specifications using Op-Amp IC 741.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors		As required
7.	Connecting wires and probes		As required

PRELAB QUESTIONS :

1. What is an inverting amplifier?
2. Which configuration of the Op-Amp is used in an inverting amplifier?
3. What is the phase difference between input and output in an inverting amplifier?
4. What is the expression for the gain of an inverting amplifier?
5. What is the function of the feedback resistor (RfR_fRf)?

THEORY:

The input signal V_i is applied to the inverting input terminal through R_1 and the non-inverting input terminal of the op-amp is grounded. The output voltage V_o is fed back to the inverting input terminal through the R_f - R_1 network, where R_f is the feedback resistor. The output voltage is given as,

$$V_o = - A_{CL} V_i$$

Here the negative sign indicates that the output voltage is 180^0 out of phase with the input signal.

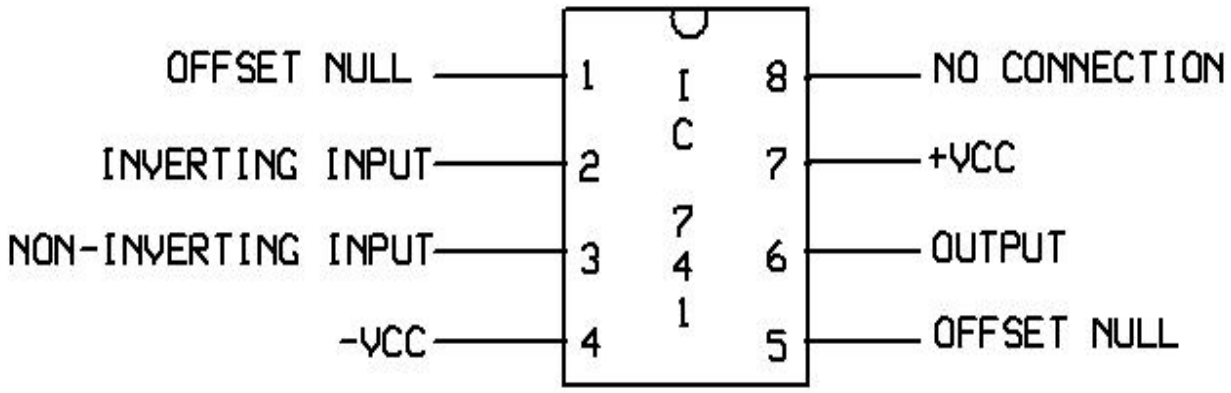
PRECAUTIONS:

1. Output voltage will be saturated if it exceeds ± 15 V.

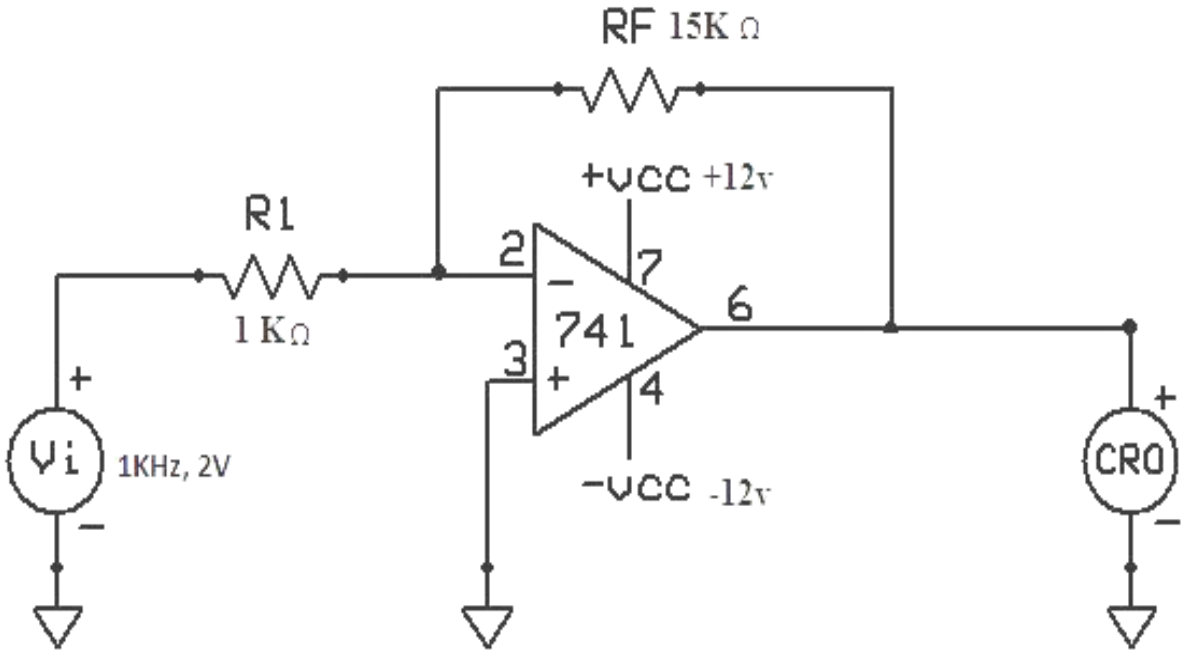
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. + V_{cc} and - V_{cc} supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.
   We know for an inverting Amplifier $A_{CL} = R_F / R_1$
   Assume R_1 (approx. 10 KΩ) and find R_f
   Hence V_O (theoretical) $= - A_{CL} V_I$

PIN DIAGRAM:



CIRCUIT DIAGRAM OF INVERTING AMPLIFIER:



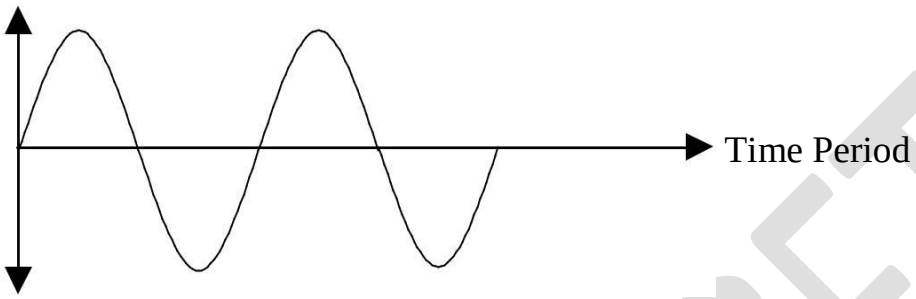
TABULATION :

OBSERVATIONS:		
S.No.	**Amplitude (No. of div x Volts per div)**	**Time period (No. of div x Time per div)**
Input		
Output	Theoretical -	
	Practical -	

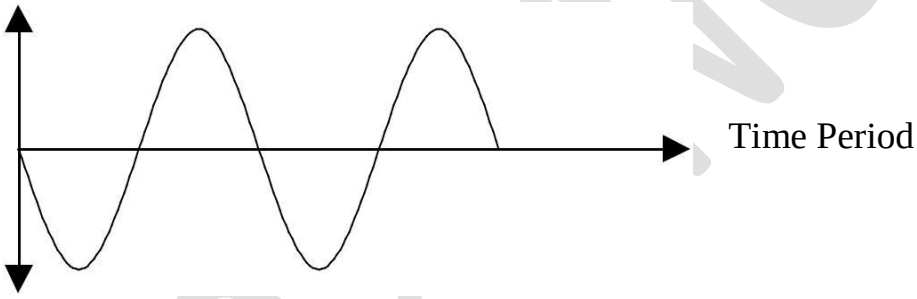
MODEL GRAPH

INVERTINGAMPLIFIER:

INPUT SIGNAL:



OUTPUT SIGNAL:



POST LAB QUESTIONS :

1. What was the objective of the experiment on the inverting amplifier?
2. How did you verify the phase inversion of the amplifier?
3. What is the role of negative feedback in an inverting amplifier?
4. How did you measure the frequency response of the amplifier?
5. Where are inverting amplifiers used in real-world applications?

RESULT:

The design and testing of the inverting amplifier is done and the input and output waveforms were drawn.

Ex.No: 9(b) **NON - INVERTING AMPLIFIER**

Date:

AIM:

To design a Non-Inverting Amplifier for the given specifications using Op-Amp IC 741.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors		As required
7.	Connecting wires and probes		As required

PRELAB QUESTIONS:

1. What is a non-inverting amplifier?
2. What is the phase difference between input and output in a non-inverting amplifier?
3. What is the formula for the voltage gain of a non-inverting amplifier?
4. What is the input impedance of a non-inverting amplifier?
5. Why is the gain of a non-inverting amplifier always greater than or equal to 1?

THEORY:

The input signal V_i is applied to the non - inverting input terminal of the op-amp. This circuit amplifies the signal without inverting the input signal. It is also called negative feedback system since the output is feedback to the inverting input terminals. The differential voltage V_d at the inverting input terminal of the op-amp is zero ideally and the output voltage is given as,

$$Vo = ACL\ Vi$$

Here the output voltage is in phase with the input signal.

PRECAUTIONS:

1. Output voltage will be saturated if it exceeds ± 15 V.

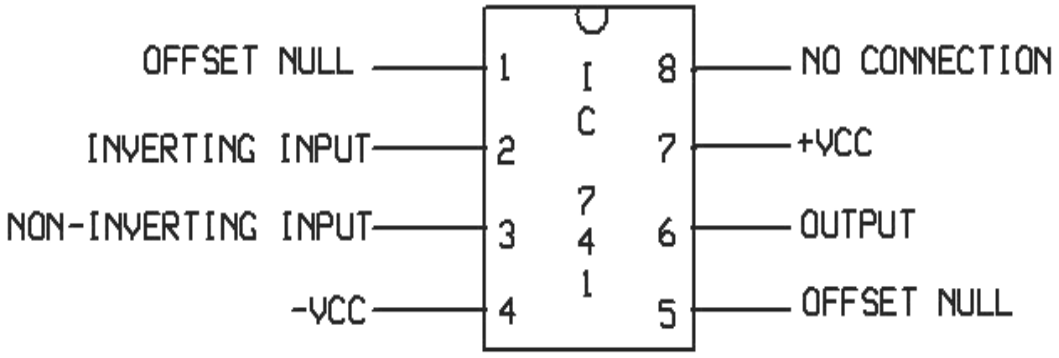
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. + V_{cc} and - V_{cc} supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the non - inverting input terminal of the Op-Amp
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

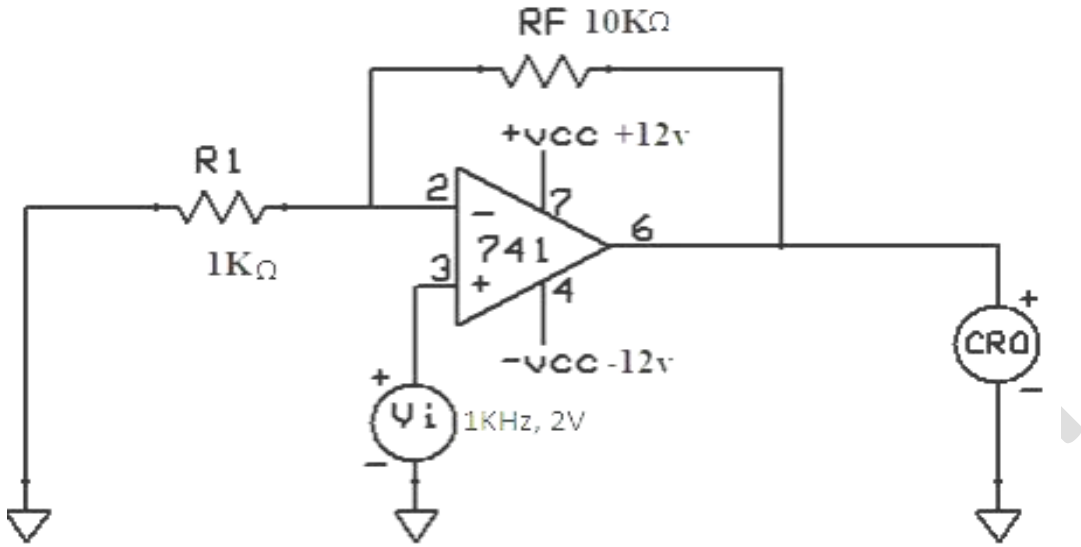
DESIGN:

We know for a Non-inverting Amplifier $A_{CL} = 1 + (R_F / R_1)$ Assume R_1 (approx. 10 KΩ) and find R_f Hence $V_o = A_{CL}\ V_i$

PIN DIAGRAM :



CIRCUIT DIAGRAM OF NON INVERITNG AMPLIFIER:



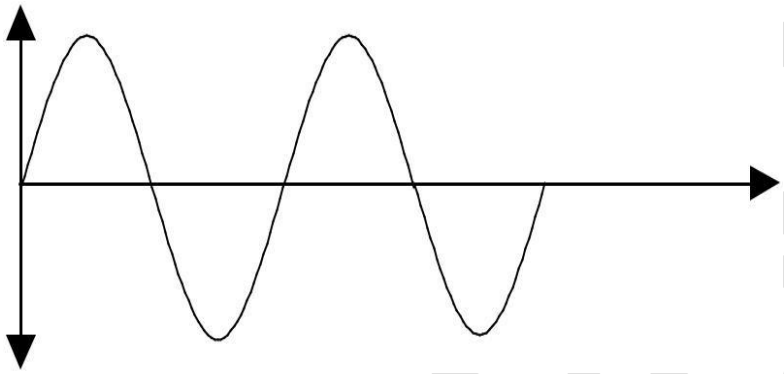
TABULATION :

S.No.	Amplitude (No. of div x Volts per div)	Time period (No. of div x Time per div)
Input		
Output	Theoretical -	
	Practical -	

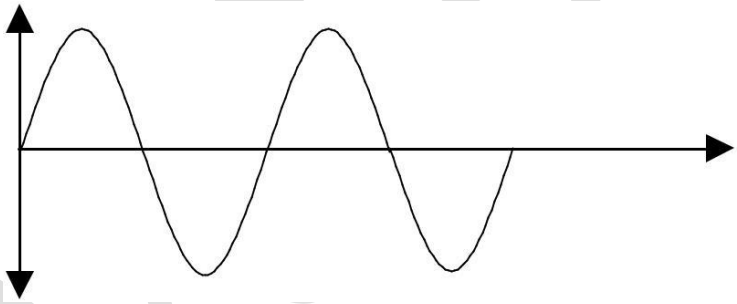
MODEL GRAPH:

NON-INVERTINGAMPLIFIER:

INPUT SIGNAL:



OUTPUT SIGNAL:



POST LAB QUESTIONS:

1. What was the objective of the experiment on the non-inverting amplifier?
2. What is the significance of negative feedback in a non-inverting amplifier?
3. What is the formula for the voltage gain of a non-inverting amplifier?
4. Why is the input impedance of a non-inverting amplifier very high?
5. What would happen if the feedback resistor RfR_fRf is removed?

RESULT:

The design and testing of the Non-inverting amplifier is done and the input and output waveforms were drawn

Ex.No:9(c) **APPLICATION OF OP-AMP**

Date: **DESIGN OF ADDER, COMPARATOR**

AIM:

a) To study the applications of IC 741 as adder and comparator.

APPARATUS REQUIRED :

1. IC 741
2. Resistors (1K□)—4
3. Function generator
4. Regulated power supply
5. IC bread board trainer
6. CRO
7. Patch cards and CRO probes

PRELAB QUESTIONS :

1. What is an adder (summing amplifier) using an Op-Amp?
2. What are the two types of adder circuits using Op-Amps?
3. What is the formula for output voltage in an inverting summing amplifier?
4. What is the formula for output voltage in a non-inverting summing amplifier?
5. Why is the output of an inverting summing amplifier negative?

THEORY:

ADDER:

Op-Amp may be used to design a circuit whose output is the sum of several input signals such as circuit is called a summing amplifier or summer. We can obtain either inverting or non inverting summer.

The circuit diagrams shows a two input inverting summing amplifier. It has two input voltages $V_1$and V_2, two input resistors R_1 ,R_2 and a feedback resistor R_f.

Assuming that op-amp is in ideal conditions and input bias current is assumed to be zero, there is no voltage drop across the resistor R_{comp} and hence the non inverting input terminal is at ground potential. By taking nodal equations.

$V_1/R_1 + V_2/R_2 + V_0/R_f = 0$

$V_0 = -[(R_f/R_1)\, V_1 + (R_f/R_2)\, V_2]$ And here

$R_1 = R_2 = R_f = 1K$

$V_0 = -(V_1 + V_2)$

Thus output is inverted and sum of input.

PRECAUTIONS:

1. Make null adjustment before applying the input signal.
2. Maintain proper Vcc levels.

PROCEDURE:

ADDER:

1. connections are made as per the circuit diagram.
2. Apply input voltage

   V_1= 5v,V_2=2v

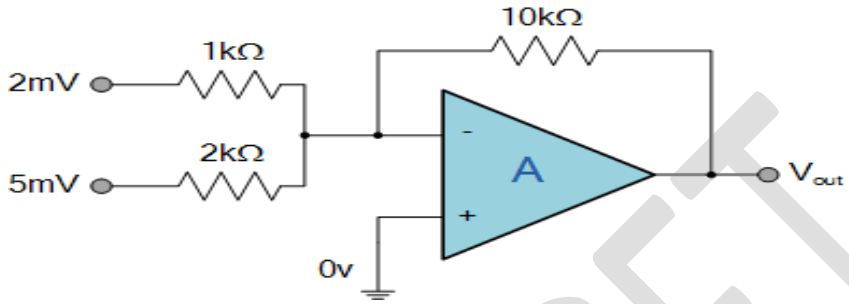
   V_1= 5v,V_2=5v 3) V_1= 5v,V_2=7v.
3. Using Millimeter measure the dc output voltage at the output terminal.
4. For different values of V_1 and V_2 measure the output voltage.

COMPARATOR:

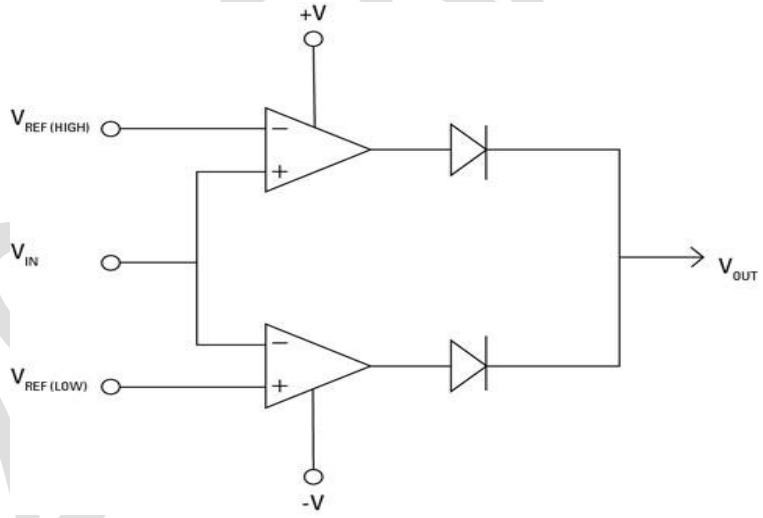
1. Connections are made as per the circuit diagram.
2. Select the sine wave of 10V peak to peak , 1K Hz frequency.
3. Apply the reference voltage 2V and trace the input and output wave forms.
4. Superimpose input and output waveforms and measure sine wave amplitude with reference to $V_{ref.}$
5. Repeat steps 3 and 4 with reference voltages as 2V, 4V, -2V, -4V and observe the waveforms.
6. Replace sine wave input with 5V dc voltage and V_{ref}= 0V.
7. Observe dc voltage at output using CRO.
8. Slowly increase V_{ref} voltage and observe the change in saturation voltage.

CIRCUIT DIAGRAM:

ADDER:



COMPARATOR:



POST LAB QUESTIONS :

1. What was the objective of the comparator experiment?
2. How does an Op-Amp function as a comparator?
3. Why do comparators operate in an open-loop configuration?
4. What are some practical applications of comparator circuits?
5. How does adding hysteresis improve comparator performance?

RESULT:

Thus the adder and comparator circuit was studied.

Ex. No: 9(d) **APPLICATIONS OF OP-AMP – II**

Date: **(DIFFERENTIATOR AND INTEGRATOR)**

.

a. DIFFERENTIATOR

AIM:

To design a Differentiator circuit for the given specifications using Op-Amp IC 741.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors		As required
7.	Capacitors		As required
8.	Connecting wires and probes		As required

POST LAB QUESTIONS :

1. What is a differentiator circuit?
2. What is the basic principle of an Op-Amp differentiator?
3. What are the types of differentiators?
4. Why is a capacitor used at the input of a differentiator circuit?
5. What is the phase shift introduced by an inverting differentiator? What is the phase shift introduced by an inverting differentiator?

THEORY:

The differentiator circuit performs the mathematical operation of differentiation; that is, the output waveform is the derivative of the input waveform. The differentiator may be constructed from a basic inverting amplifier if an input resistor R_1 is replaced by a capacitor C_1. The expression for the output voltage is given as, $V_o = - R_f C_1 (dV_i /dt)$

Here the negative sign indicates that the output voltage is 180 ^{0} out of phase with the input signal. A resistor $R_{comp} = R_f$ is normally connected to the non-inverting input terminal of the op-amp to compensate for the input bias current. A workable differentiator can be designed by implementing the following steps:

1. Select f_a equal to the highest frequency of the input signal to be differentiated. Then, assuming a value of $C_1 < 1$ µF, ca lculate the value of R_f.

2. Choose $f_b = 10\ f_a$ and calculate the values of R_1 and C_f so that $R_1C_1 = R_f\ C_f$.

3. The differentiator is most commonly used in waveshaping circuits to detect high frequency components in an input signal and also as a rate–of–change detector in FM modulators.

PROCEDURE:

1. Connections are given as per the circuit diagram.
2. $+ V_{cc}$ and $- V_{cc}$ supply is given to the power supply terminal of the Op-Amp IC.
3. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.
4. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.

DESIGN:

Given $f_a = 1$KHz

We know the frequency at which the gain is 0 dB, $f_a = 1 / (2\pi R_f C_1)$ Let us assume $C_1 = 0.01$ µF; then

$R_f = 1/(2\pi(1 \times 10^3)(0.01 \times 10^{-6})) = 15.9K\Omega \approx 15K\Omega$

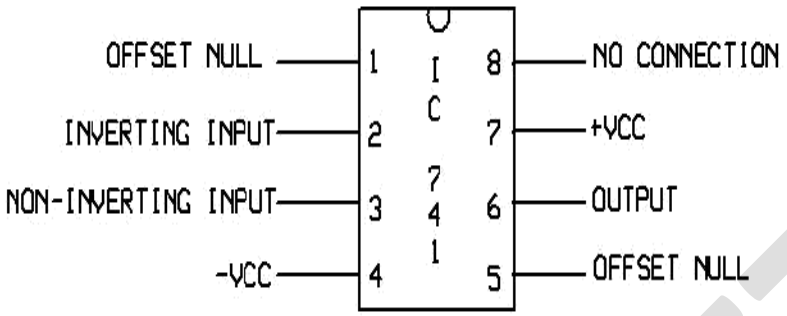
Since $f_b = 10\ f_a$, $f_b = 10$ KHz

We know that the gain limiting frequency $f_b = 1 / (2\pi R_1 C_1)$ Hence $R_1 = 1 /(2\pi(10 \times 10^3)(0.01 \times 10^{-6})) = 1.59\ K\Omega \approx 1.5K\Omega$

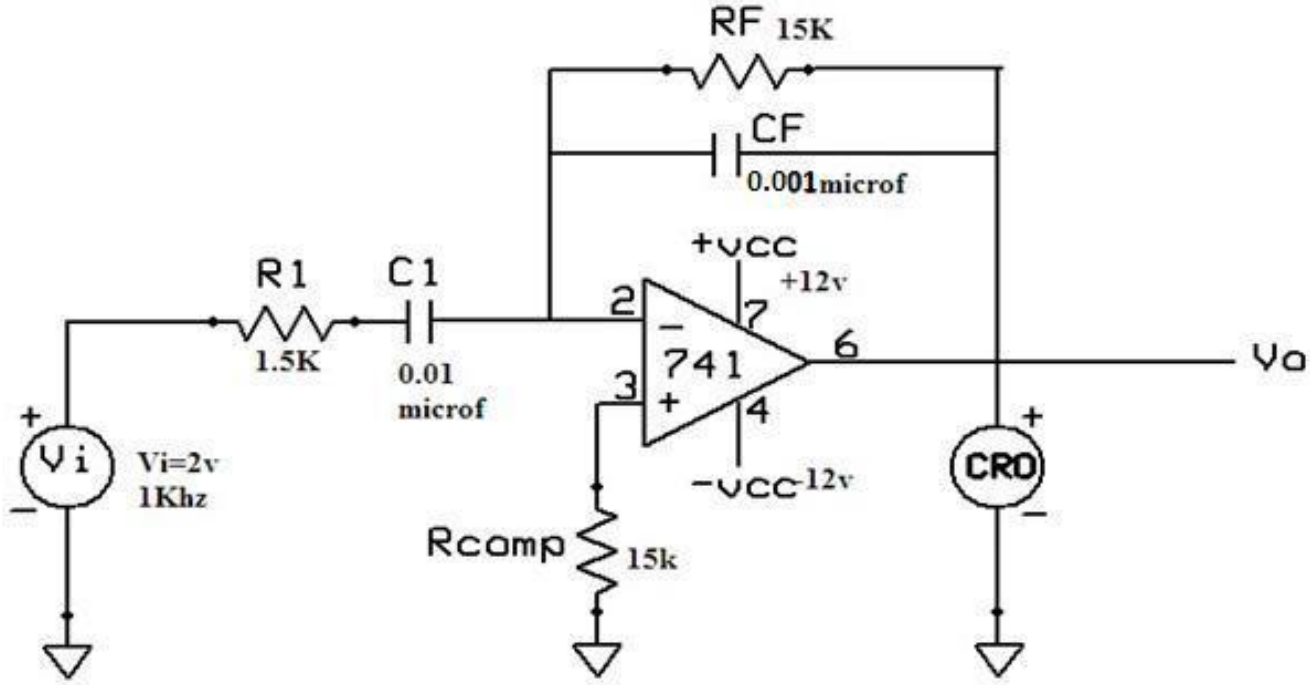
Also since $R_1C_1 = R_f C_f$; $C_f = R_1C_1 / R_f$

$C_f = (1.5 \times 10^3 \times 0.01 \times 10^{-6}) / (15 \times 10^3) = 0.001$ µF

PIN DIAGRAM:



CIRCUIT DIAGRAM OF DIFFERENTIATOR:



TABULATIONS:

INPUT - SINE WAVE

S.No.	Amplitude (No. of div x Volts per div)	Time period (No. of div x Time per div)
Input		
Outut		

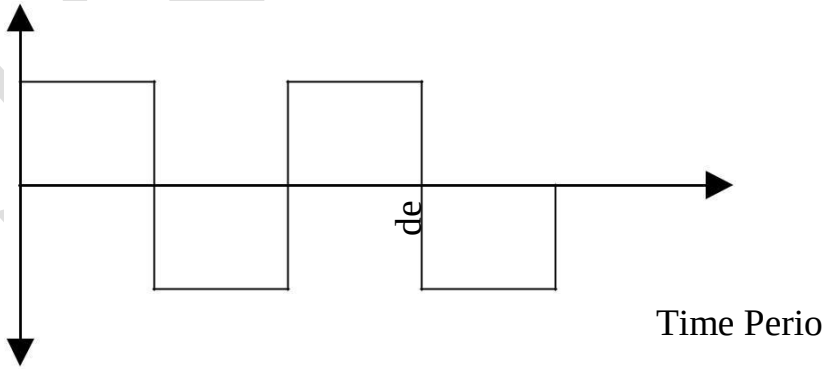
INPUT – SQUARE WAVE

S.No.	Amplitude (No. of div x Volts per div)	Time period (No. of div x Time per div)
Input		
Outut		

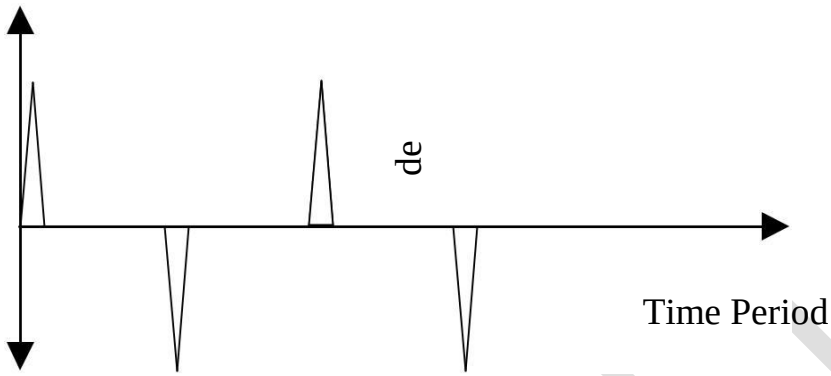
MODEL GRAPH:

DIFFERENTIATOR:

INPUT SIGNAL:



OUTPUT SIGNAL:



POST LAB QUESTIONS :

1. What was the objective of the differentiator experiment?
2. What mathematical expression governs the operation of a differentiator?
3. What kind of input waveform gives the highest output voltage in a differentiator?
4. How did you reduce noise effects in your differentiator circuit?
5. Why did we use an operational amplifier instead of a simple RC differentiator?

RESULT:

The design of the Differentiator circuit was done and the input and output waveforms were obtained

Ex.No:9(e) **INTEGRATOR**

Date:

AIM:

To design an Integrator circuit for the given specifications using Op-Amp IC 741.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Function Generator	3 MHz	1
2.	CRO	30 MHz	1
3.	Dual RPS	0 – 30 V	1
4.	Op-Amp	IC 741	1
5.	Bread Board		1
6.	Resistors		As required
7.	Capacitors		As required
8.	Connecting wires and probes		As required

PRELAB QUESTIONS:

1. What is an integrator circuit?
2. What is the basic principle of an Op-Amp integrator?
3. Why is a capacitor used in an integrator circuit?
4. What is the difference between an ideal and a practical integrator?
5. What is the phase shift introduced by an inverting integrator?

THEORY:

A circuit in which the output voltage waveform is the integral of the input voltage waveform is the integrator. Such a circuit is obtained by using a basic inverting amplifier configuration if the feedback resistor R_f is replaced by a capacitor C_f. The expression for the output voltage is given as,

$$V_o = - (1/R_f C_1) \int V_i \, dt$$

Here the negative sign indicates that the output voltage is 180^0 out of phase with the input signal. Normally between f_a and f_b the circuit acts as an integrator. Generally, the

value of $f_a > f_b$. The input signal will be integrated properly if the Time period T of the signal is larger than or equal to $R_f C_f$. That is,

$$T \geq R_f C_f$$

The integrator is most commonly used in analog computers and ADC and signal-wave shaping circuits.

PROCEDURE:

1. Connections are given as per the circuit diagram.
2. $+ V_{cc}$ and $- V_{cc}$ supply is given to the power supply terminal of the Op-Amp IC.
3. The output voltage is obtained in the CRO and the input and output voltage waveforms are plotted in a graph sheet.
4. By adjusting the amplitude and frequency knobs of the function generator, appropriate input voltage is applied to the inverting input terminal of the Op-Amp.

DESIGN:

Given $f_a = 10KHz$

We know the frequency at which the gain is 0 dB, $f_a = 1 / (2\pi R_1 C_f)$

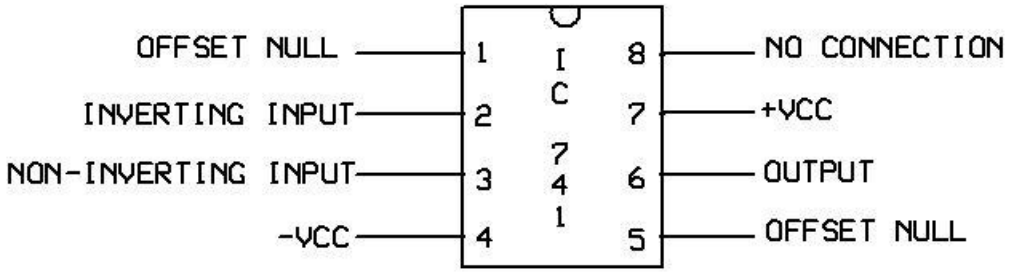
Therefore fb = 10KHz Since $f_b = 0.1 f_a$, and

also the gain limiting frequency $f_b = 1 / (2\pi R_f C_f)$, assume $C_f = 0.01\mu F$

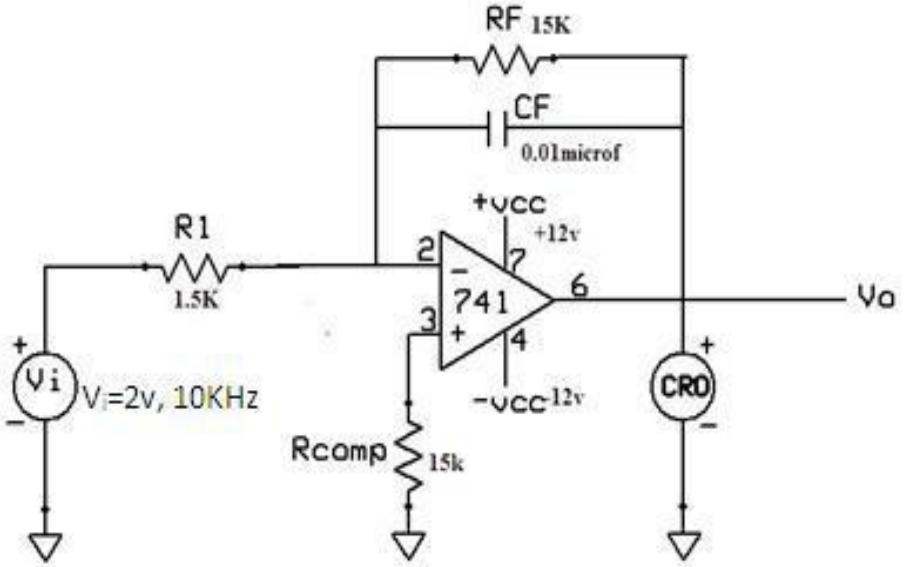
$R_f = 1 /(2\pi (1000)(0.01 \times 10^{-6}) = 15.9\ K\Omega \approx 15K\Omega$

$R_1 = 1/(2\ \pi\ (10000)\ (0.01 \times 10^{-6}) = 1.59\ K\Omega \approx 1.5K\Omega$

PIN DIAGRAM:



CIRCUIT DIAGRAM OF INTEGRATOR:



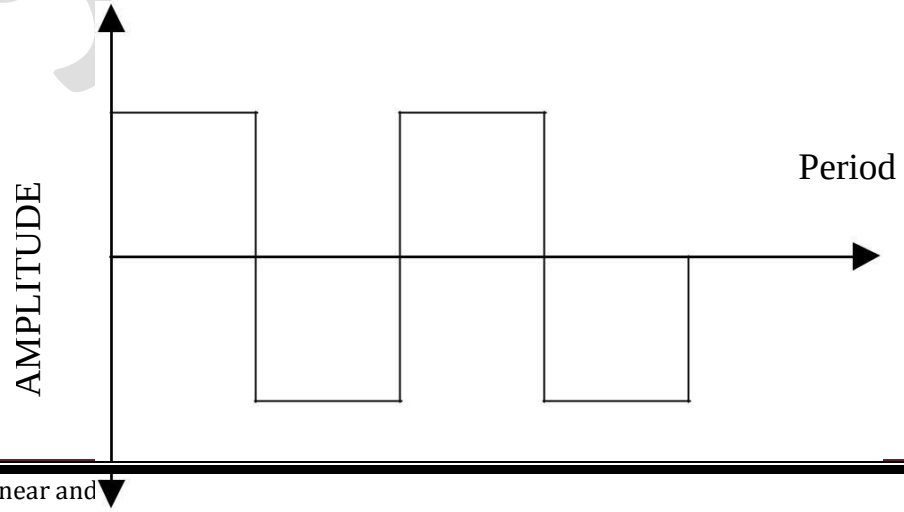
TABULATIONS :

S.No.	Amplitude (No. of div x Volts per div)	Time period (No. of div x Time per div)
Input		
Output		

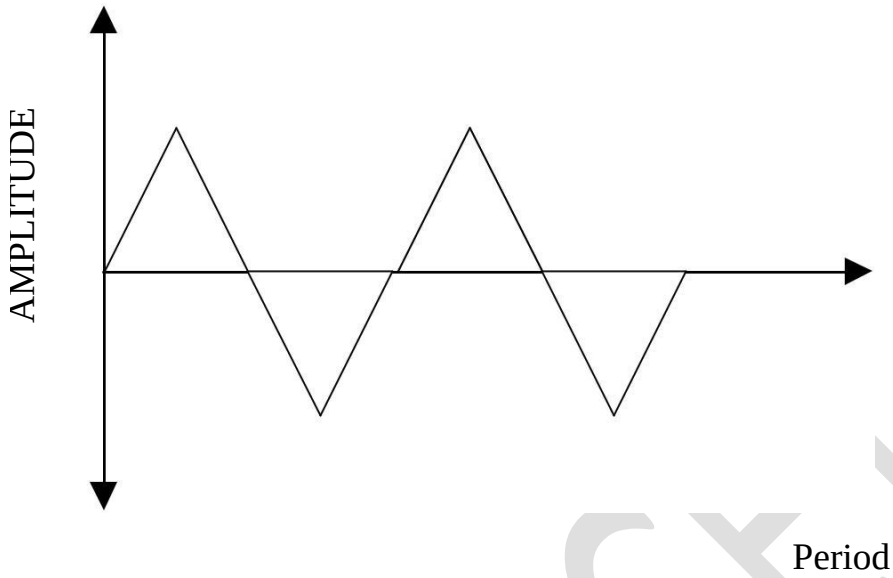
MODEL GRAPH:

INTEGRATOR:

INPUT SIGNAL:



OUTPUT SIGNAL:



POST LAB QUESTIONS:

1. What was the objective of the integrator experiment?
2. How did you verify the working of the integrator circuit in the experiment?
3. Why is a practical integrator preferred over an ideal integrator in real applications?
4. What was the role of the feedback capacitor in the integrator circuit?
5. How does the integrator behave at very high frequencies?

RESULT:

The design of the Integrator circuit was done and the input and output waveforms were obtained.

EX-NO:10 STUDY OF VCO AND PLL ICS

DATE :

AIM :

i. To study the Voltage to frequency characteristics of NE/ SE 566 IC.

PRELAB QUESTIONS:

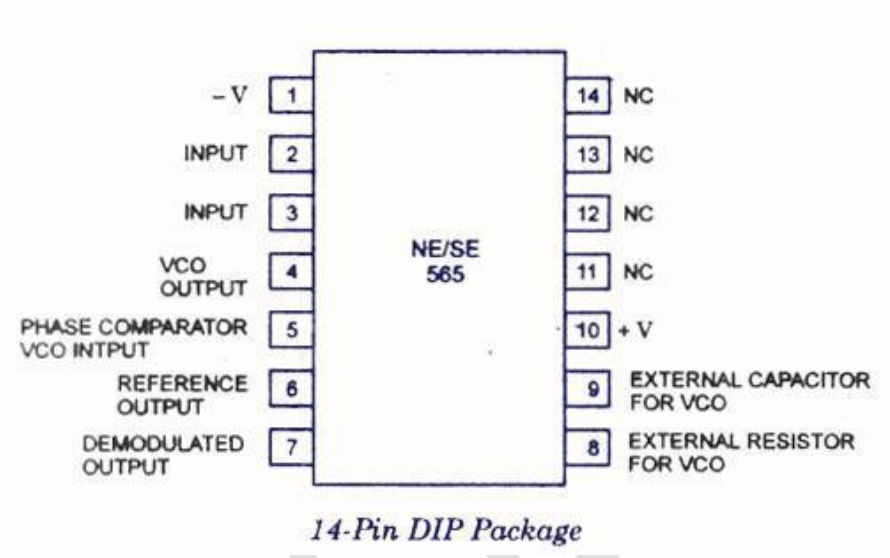
1. What is a voltage-to-frequency converter (VFC)?
2. What is the basic principle behind voltage-to-frequency conversion?
3. What is the output of a voltage-to-frequency converter?
4. What type of components are commonly used in voltage-to-frequency conversion circuits?
5. What is the general formula relating output frequency and input voltage in a VFC?

THEORY:

INTRODUCTION TO PLL OR PHASE LOCKED LOOPS

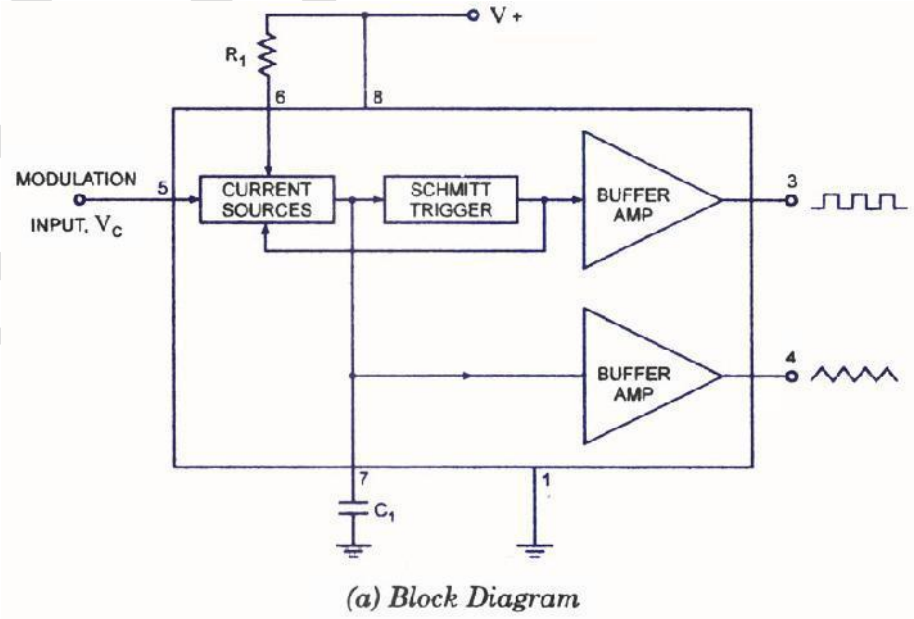
Phase-locked loop is a feedback loop consisting of a phase detector, a low-pass filter, amplifier (optional) and a voltage-controlled oscillator (VCO), as illustrated in figure. It plays the same role in the frequency or phase world as the op-amp does in the voltage world. The op-amp has two voltage inputs, non-inverting and inverting (normally used for feedback from the output). Similarly, the PLL has two inputs; the PLL's feedback input is normally connected to the circuits' output. Digital frequencies are usually applied. The op-amp changes its output voltage to whatever values is necessary to drive the difference in voltage between its two inputs to zero. The PLL changes its output phase and frequency to whatever frequency or phase is necessary to make the two input frequencies and phase track. Placing a voltage divider in the feedback loop of an op-amp causes the output voltage to be increased by the amount of the feedback voltage division (amplification). Placing a frequency divider in the feedback of a PLL causes the output frequency to be increased by the amount of the feedback divider. A firm grasp on similarities between the PLL and the op-amp simplifies our analysis and design of circuits containing PLLs.

PLL PIN DIAGRAM :

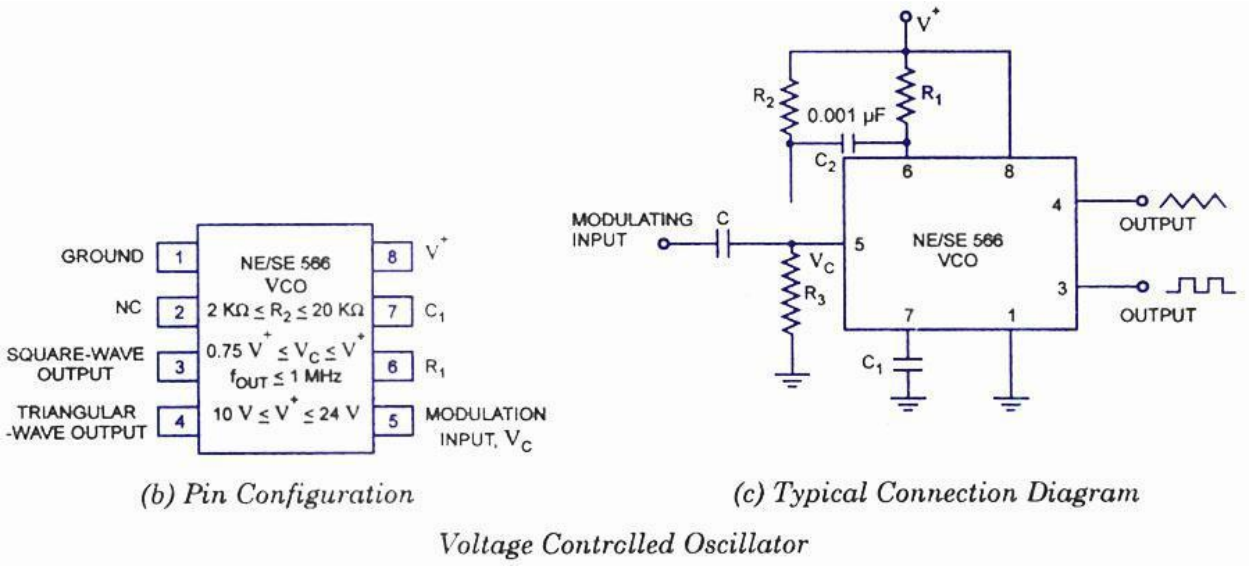


14-Pin DIP Package

VOLTAGE CONTROLLED OSCILLATOR



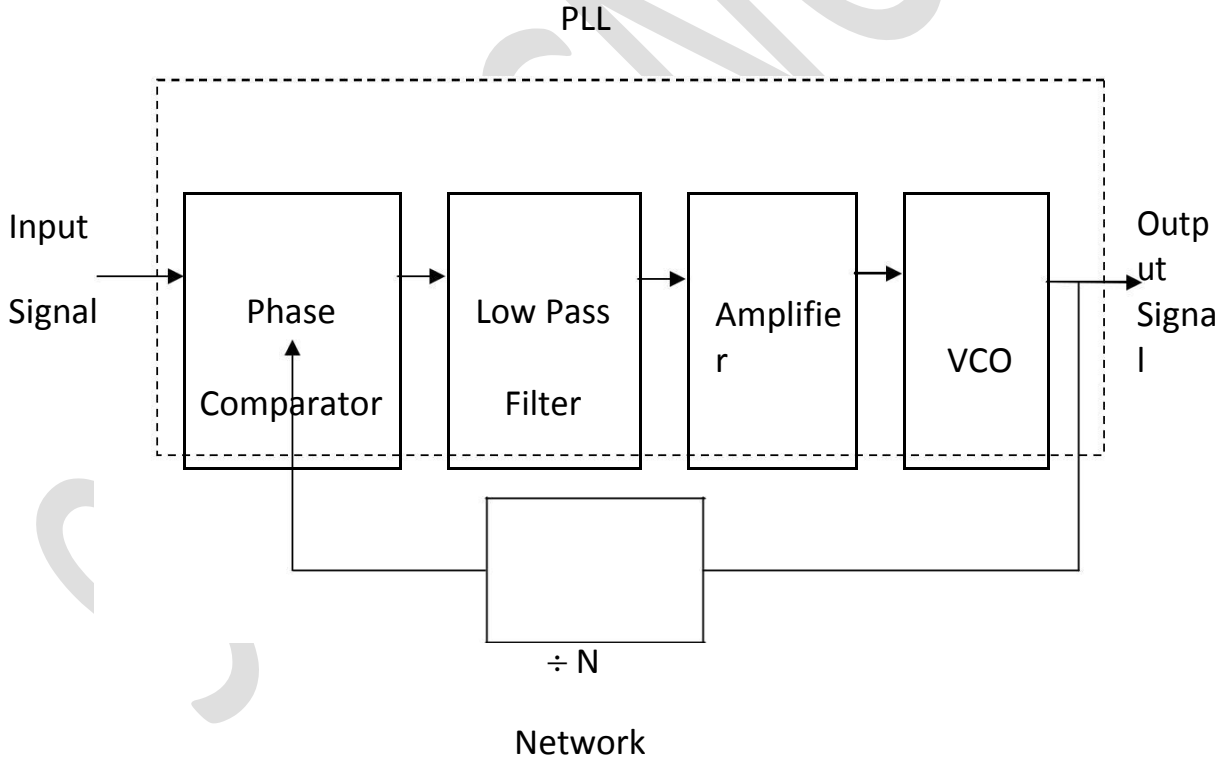
(a) Block Diagram



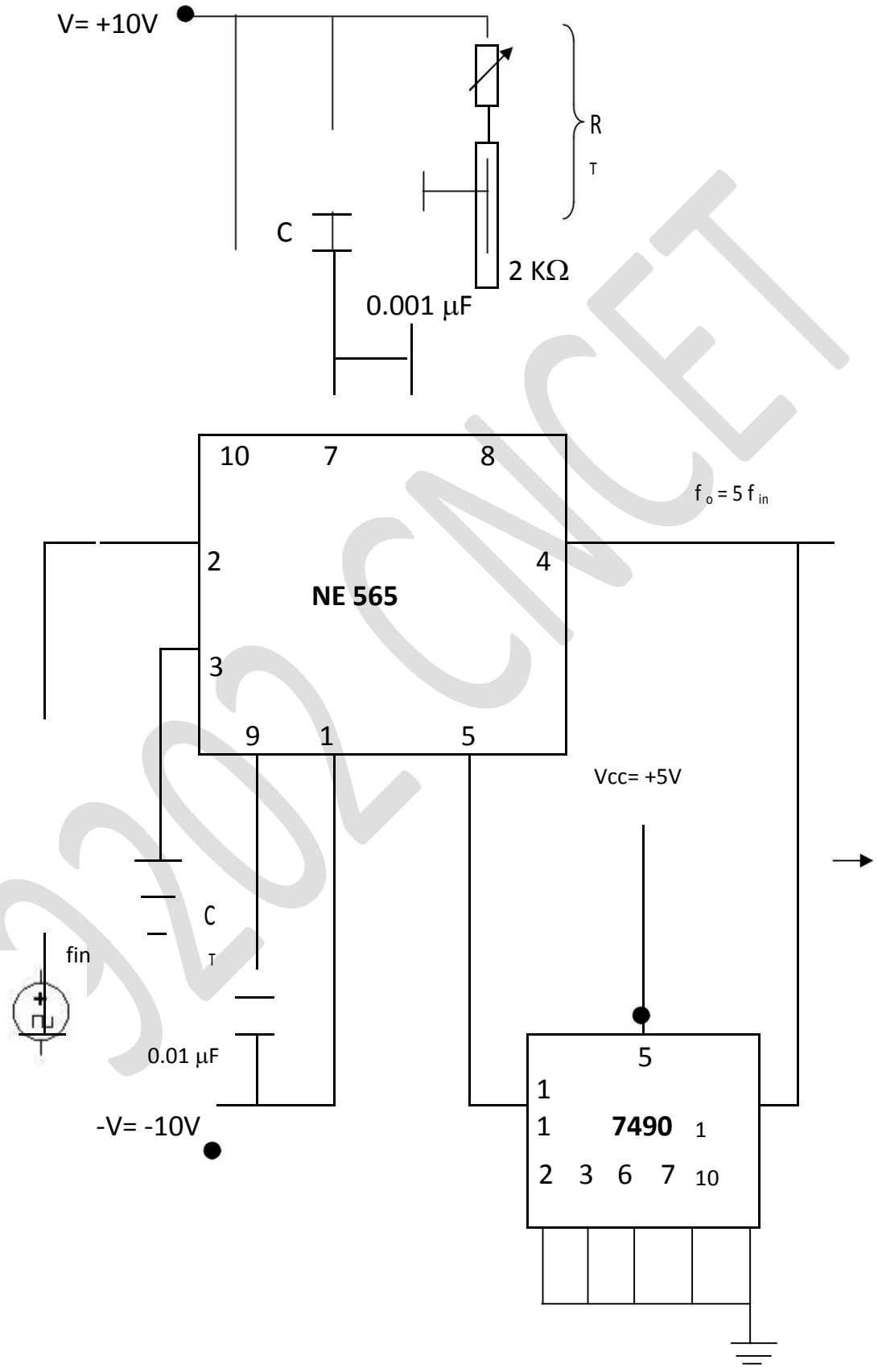
(b) Pin Configuration *(c) Typical Connection Diagram*

Voltage Controlled Oscillator

BLOCK DIAGRAM:



CIRCUIT DIAGRAM:



POST LAB QUESTIONS:

1. How does temperature affect the performance of a VFC?
2. What is the importance of linearity in a VFC?
3. How does temperature affect the performance of a VFC?
4. How does increasing the input voltage affect the output of a VFC?
5. What role does a feedback resistor play in a VFC circuit?

RESULT:

Thus the design, construction of variable voltage to frequency of NE/SE566 IC characteristics is obtained

Ex. No:11 VARIABILITY VOLTAGE REGULATOR USING IC LM317

Date:

AIM:

To design and test the power supply using LM317.

APPARATUS REQUIRED:

S. No	Name of The Apparatus	Specification	Quantity
1	LM317	-	1
3	Resistor	1.4K, 1K,,1.6K	1
4	Resistor	10K	2
5	Capacitor	0.1µF,100pF,330 µF,22 µF	1
6	DRB	-	1
7	CRO	-	1
8	Bread board	-	-

PRELAB QUESTIONS:

1. What is the function of a voltage regulator?
2. Why is LM317 called an adjustable voltage regulator?
3. What are the three terminals of the LM317?
4. What is the output voltage range of LM317?
5. What is the function of the adjust pin in LM317?

THEORY :

A variable voltage regulator is a circuit that provides an adjustable output voltage based on the user's requirements. The LM317 is a widely used adjustable voltage regulator that can output voltages from 1.25V to 37V with a maximum output current of 1.5A.

The LM317 is a three-terminal adjustable voltage regulator with:

- Input Voltage (Vin)
- Output Voltage (Vout)

- Adjustment Pin (Adj)

Unlike fixed voltage regulators like LM7805 or LM7812, which provide a constant voltage output, the LM317 allows users to adjust the output voltage using an external resistor divider network.

- ❖ Input Voltage (Vin): A DC voltage higher than the required output is applied to the Vin pin.
- ❖ Voltage Adjustment: The resistor divider R1R_1R1 and R2R_2R2 sets the output voltage by controlling the adjustment pin.
- ❖ Output Regulation: The LM317 maintains a constant output voltage despite fluctuations in input voltage or load.

PROCEDURE :

LM317:

i) Connections are made as per the circuit diagram

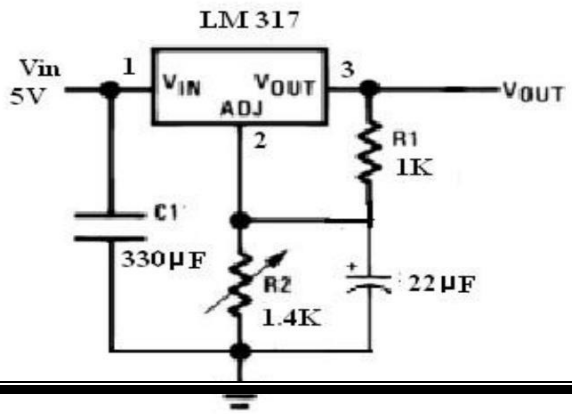
ii) Set up the input voltage as 5V,6V and 10V

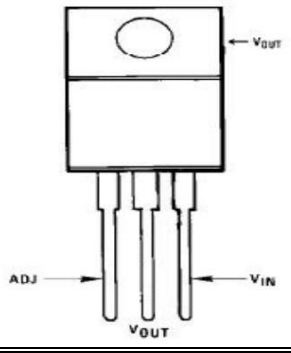
iii) Vary the resistance R_2 (designing value) the corresponding output voltage are noted down.

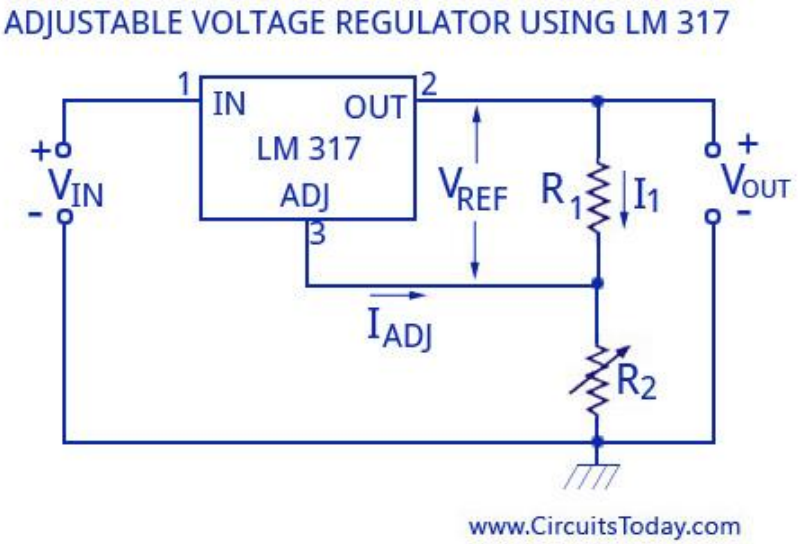
iv) Plot the graph between resistance R_2 and the observed output voltage

CIRCUIT DIAGRAM :

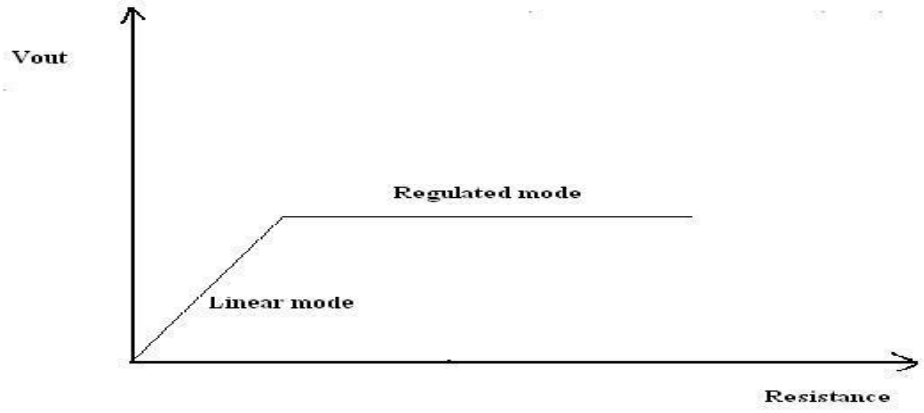
LM317:






ADJUSTABLE VOLTAGE REGULATOR USING LM 317
1
IN
OUT
2
LM 317
ADJ
3
+
VIN
-
VREF
R1
I1
+
VOUT
-
IADJ
R2
www.CircuitsToday.com

MODEL GRAPH:


Vout
Regulated mode
Linear mode
Resistance

POST LAB QUESTIONS :

1. What are the input and output voltage limits for LM317?
2. What is the formula to calculate the output voltage of LM317?
3. Why do we use capacitors in the LM317 circuit?
4. What is the role of the adjust pin in LM317?
5. What is the minimum load current for LM317?

RESULT:

To design and test the DC power supply using LM317was done and wave form were obtained

VALUE ADDED EXPERIMENTS

Ex. No:12 INSTRUMENTATION AMPLIFIER

Date:

AIM:

To design an instrumentation amplifier and obtain the output for various gain.

APPARATUS REQUIRED:

S.NO.	COMPONENTS NAME	SPECIFICATION & RANGE	QUANTITY
1.	Bread board	-	1
2.	Op amp	IC741	3
3.	Function generator	3 MHz	2
4.	CRO	30 MHz	1
5.	Dual power supply	+12/-12V	1
6.	Resistors		Each 1
7.	Connecting wires	Single strand	As required

PRE LAB QUESTIONS:

1. What is an Instrumentation amplifier?
2. What are the advantages of instrumentation amplifier?
3. What are the Applications of Instrumentation Amplifier?
4. Difference between Operational Amplifier and Instrumentation Amplifier
5. What are the features of instrumentation amplifier?

THEORY:

Instrumentation amplifier is a kind of differential amplifier with additional input buffer stages. The addition of input buffer stages makes it easy to match (impedance matching) the amplifier with the preceding stage. Instrumentation are commonly used in industrial test and measurement application. The instrumentation amplifier also has some useful features like low offset voltage, high CMRR (Common mode rejection ratio), high input resistance, high gain etc.

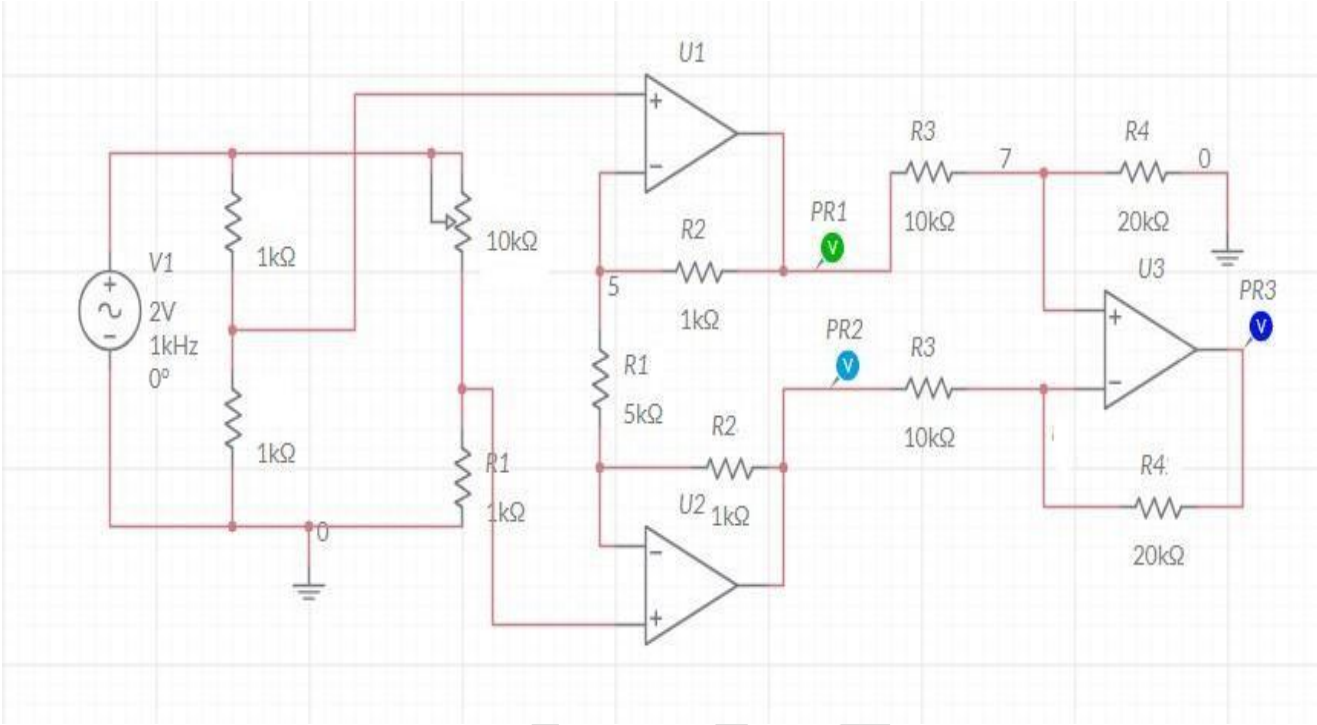
The two non-inverting amplifiers form a differential input stage acting as buffer amplifiers with a gain of 1 + 2R2/R1 for differential input signals and unity gain for common mode input signals.

Since amplifiers A1 and A2 are closed loop negative feedback amplifiers, we can expect the voltage at Va tobe equal to the input voltage V1. Likewise, the voltage at Vb to be equal to the value at V2.

As the op-amps take no current at their input terminals (virtual earth), the same current must flow through the three resistor network of R2, R1 and R2 connected across the op-amp outputs. This means then that the voltage on the upper end of R1 will be equal to V1and the voltage at the lowerend of R1 to be equal to V2.

The voltage output from the differential op-amp A3 acting as a subtractor, is simply the difference between its two inputs (V2 – V1) and which is amplified by the gain of A3which may be one, unity,(assuming that R3 = R4).

CIRCUIT DIAGRAM:



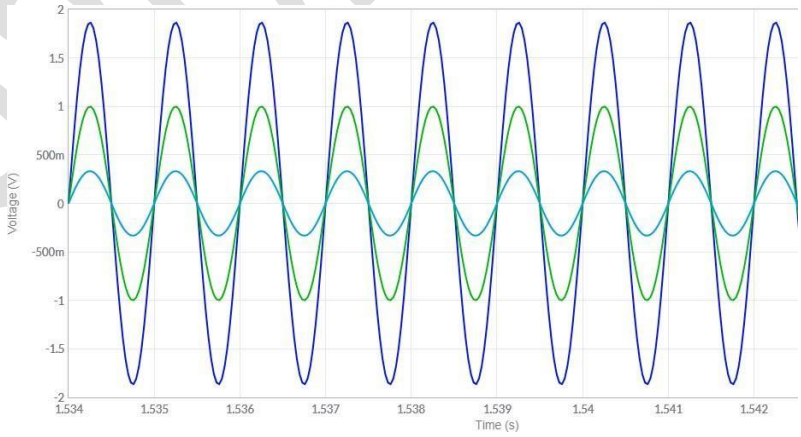
PROCEDURE:

1. Connections are given as per the circuit diagram.
2. Input signal is connected to the circuit from the signal generator.
3. The input and output signals of the circuit observed from the dual channels 1 and 2 of theCRO.
4. Suitable voltage sensitivity and time-base on CRO is selected.
5. Change the gain setting resistor value and observe the output.

TABULATION:

Input /Output	Theoretical			Practical		
	Amplitude	Time				
Input						
Output	V1	V2	Vo	V1	V2	Vo

OUTPUT:



POST LAB QUESTIONS:

1. In an instrumentation amplifier using transducer bridge, which device measure the change in physical energy ?
2. Which IC is used for Instrumentation amplifier?
3. What are the types of Instrumentation amplifier?
4. What are 2 modes of Operation in Instrumentation amplifier?
5. What are the roles of analog amplifiers in various electronic devices.

RESULT:

Thus the Instrumentation amplifier was designed and verified.

Ex.No:12 **SIMULATION USING SPICE (USING TRANSISTOR)**

Date: **BISTABLE MULTIVIBRATOR**

AIM :

To construct and simulate the Bistable multivibrator by using pspice.

SOFTWARE USED

Multisim 13.0

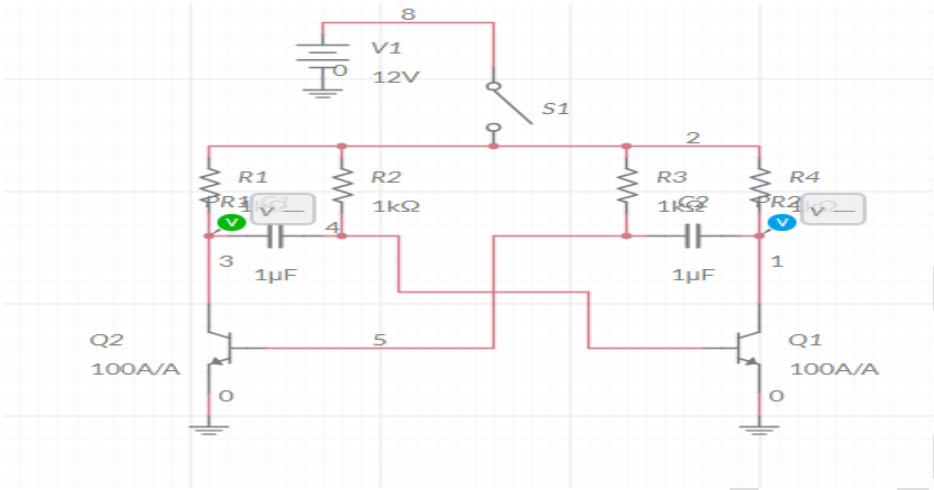
PRELAB QUESTIONS:

1. What is Multivibrator?
2. What are the other names of Bistable Multivibrator?
3. Mention the names of different kinds of triggering used in the circuit shown?
4. What is a stable state?
5. Describe the principle of fixed-bias Binary?

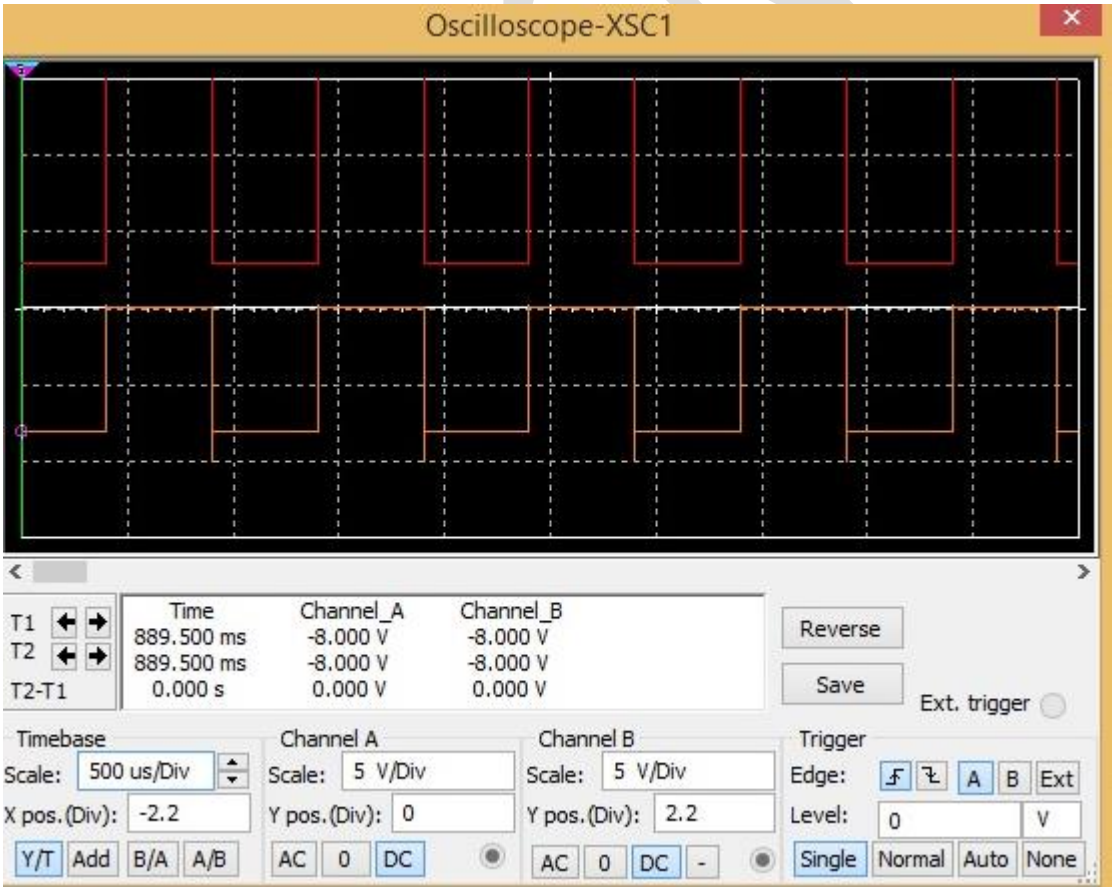
PROCEDURE :

1. Open Multisim and create a "design".
2. Draw a schematic diagram of the circuit (components and interconnections).
3. Connect signal sources to the circuit inputs , then stimulate the circuit to produce the output .
4. Connect the circuit outputs to one or more indicators to display the response of the circuit
5. Run the simulation and examine the results, copying and pasting Multisim windows into lab reports and other documents as needed.
6. Save the design.

CIRCUIT DIAGRAM:



OUTPUT WAVEFORM:



POST LAB QUESTIONS :

1. What is staggered tuned amplifier?
2. Q factor Provides?
3. Why Q factor is kept as high as possible in tuned circuits?
4. What are the advantages of staggered tuned amplifier?
5. What is the need of neutralization in tuned amplifiers?

RESULT:

Thus the Bistable Multivibrator circuit was designed and simulated using pspice simulator .